

Hawke Intel Discrete Block Diagram

CLK GEN
ICS9LPRS365

Intel Mobile CPU

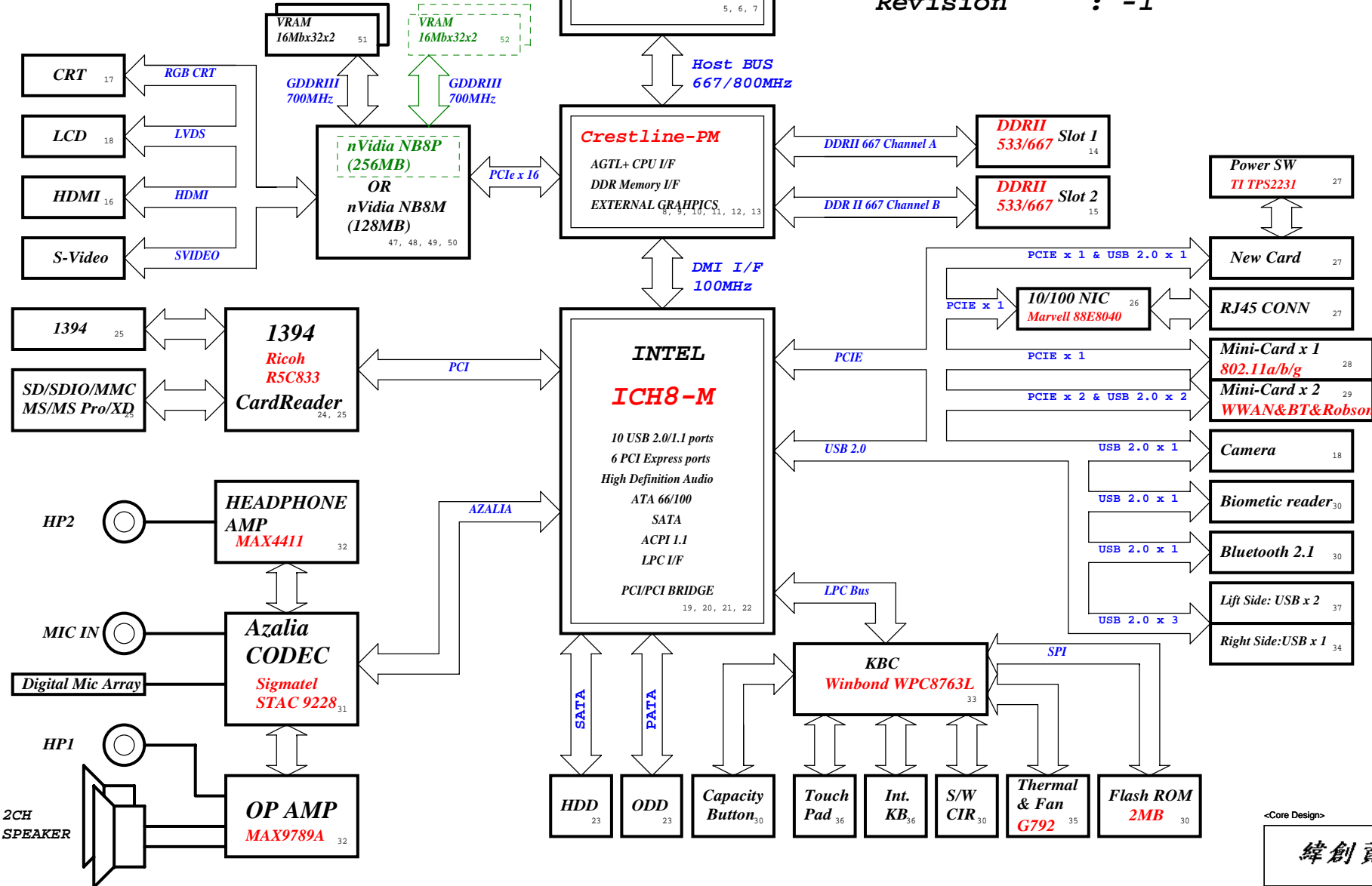
Merom 4M
FSB:667 or 800 MHz

Project code : 91.4W101.001

PCB P/N : 48.4W101.011

PCB No. : 07212

Revision : -1



BATTERY CHARGER MAX8731A		38
INPUTS	OUTPUTS	
AD+ BAT+	DCBATOUT	
SYSTEM DC/DC TPS51120		39
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
SYSTEM DC/DC TPS5117		42, 43
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0 1D8V_S3	
SYSTEM DC/DC TPS51100		44
INPUTS	OUTPUTS	
1D8V_S3	0D9V_S3	
SYSTEM DC/DC RT9018		44
INPUTS	OUTPUTS	
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0	
VGA DC/DC TPS5117		53
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFX_CORE_S0	
CPU DC/DC ISL6262A		40
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
PCB LAYER		
L1:TOP		
L2:GND		
L3:Signal		
L4:Signal		
L5:VCC		
L6:Singal		
L7:GND		
L8:BOT		

<Core Design>

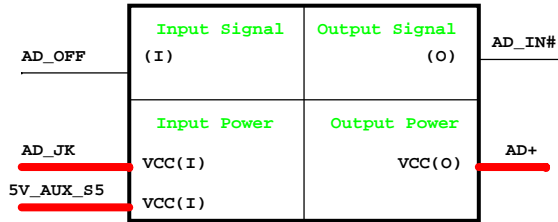
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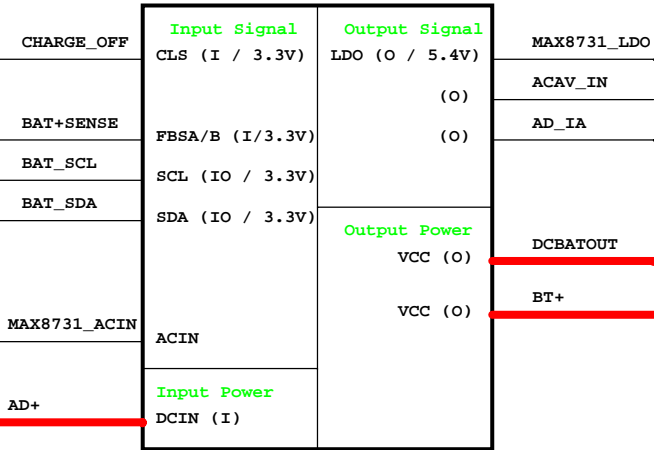
System Block Diagram		
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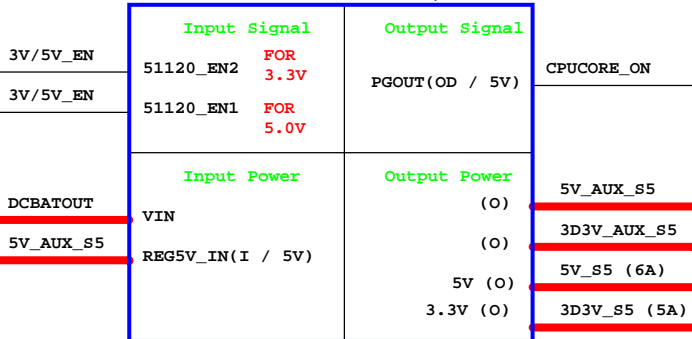
Adapter



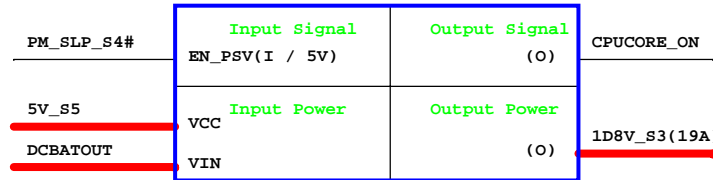
Charger MAX8731A



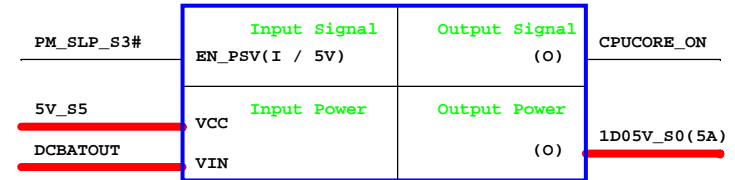
TI TPS51120 3D3V/5V



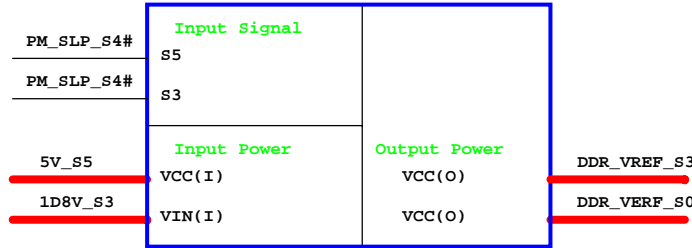
TPS51117 1D8V



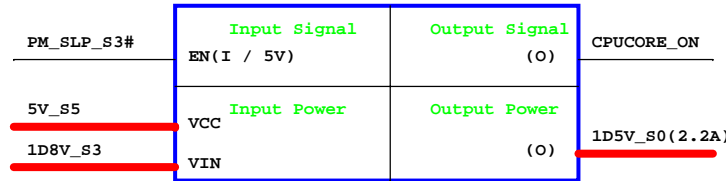
TPS51117 1D05V



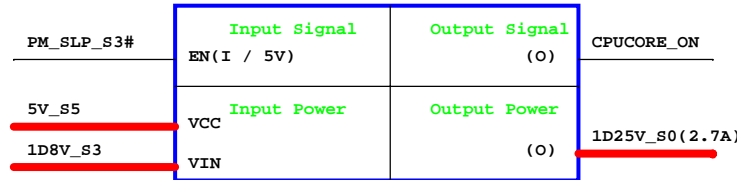
TI TPS51100 0.9V/DDR_VREF_S3



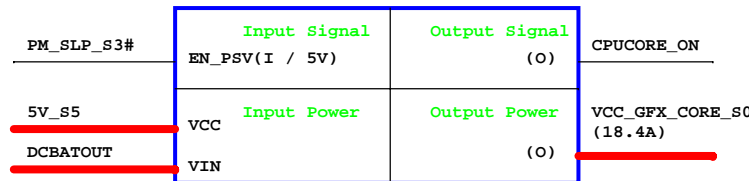
RT9018A 1D5V



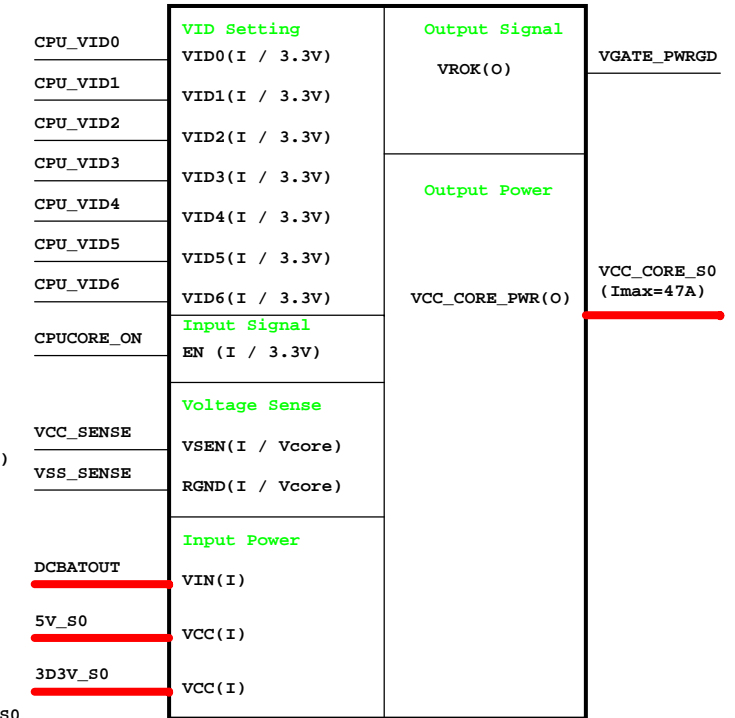
RT9018A 1D25V



TPS51117 VGA_CORE



ISL6262A CPU_CORE



<Core Design>

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Title		
Power Block Diagram		
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP_Tp3	AZ_DOUT_ICH	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation(default)	
1	1	Set PCIE port config bit1	

A16 swap override strap		
PCI_GNT#3	low = A16_swap_override_enable	
	high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

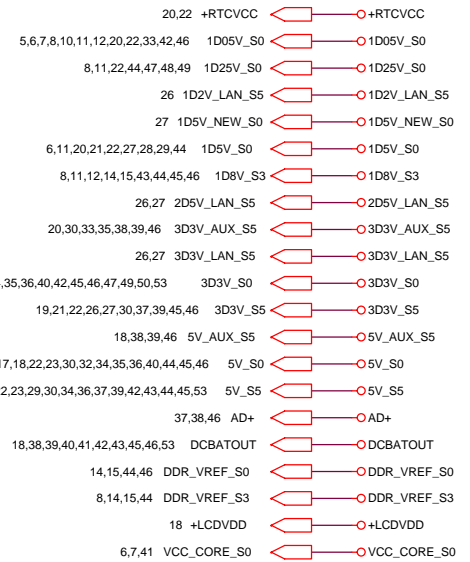
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CI_RST#	TBD



PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

<Core Design>

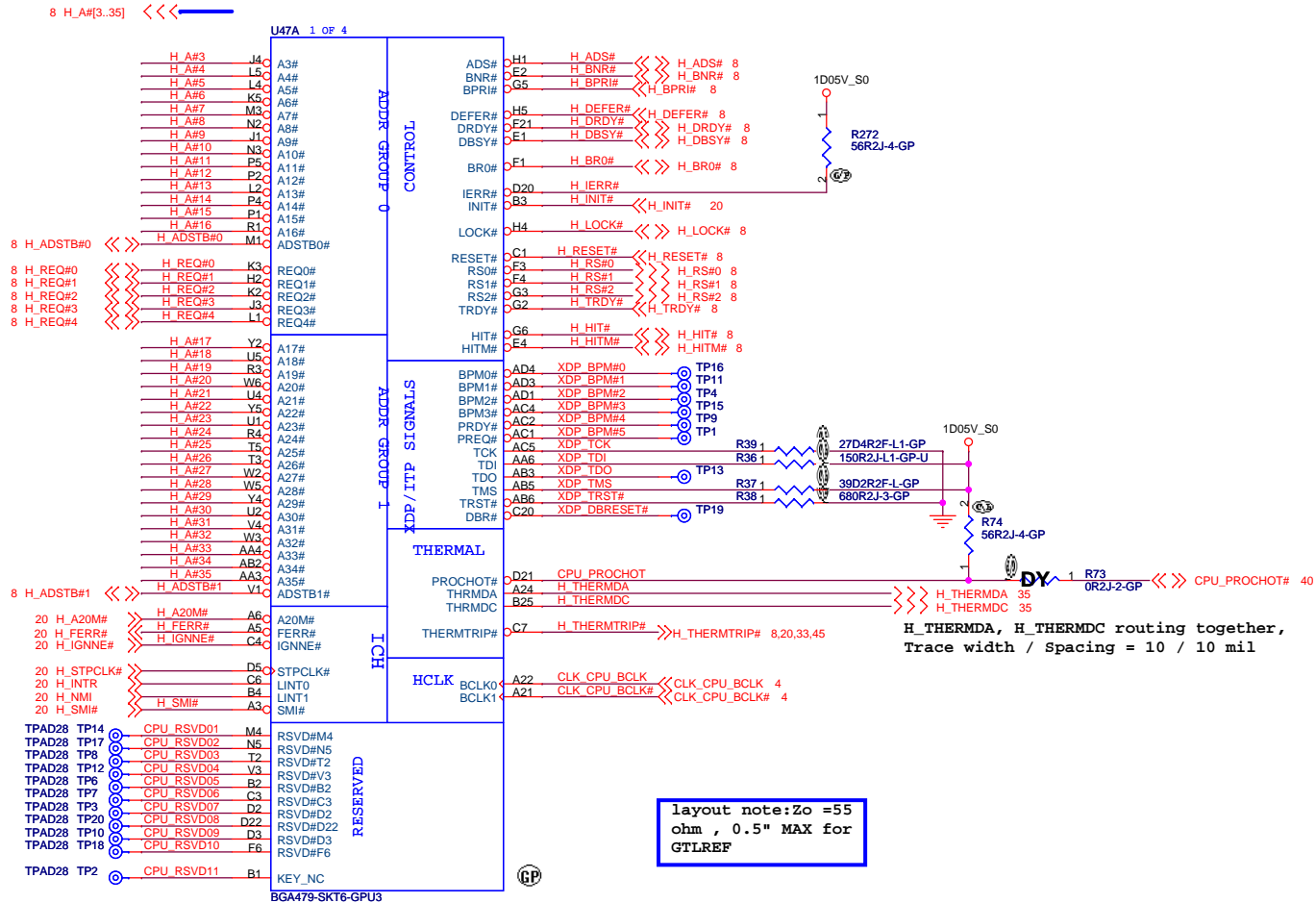
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INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled★
CFG 19 DMI Lane Reserved	Normal Operation★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present★	SDVO Card Present

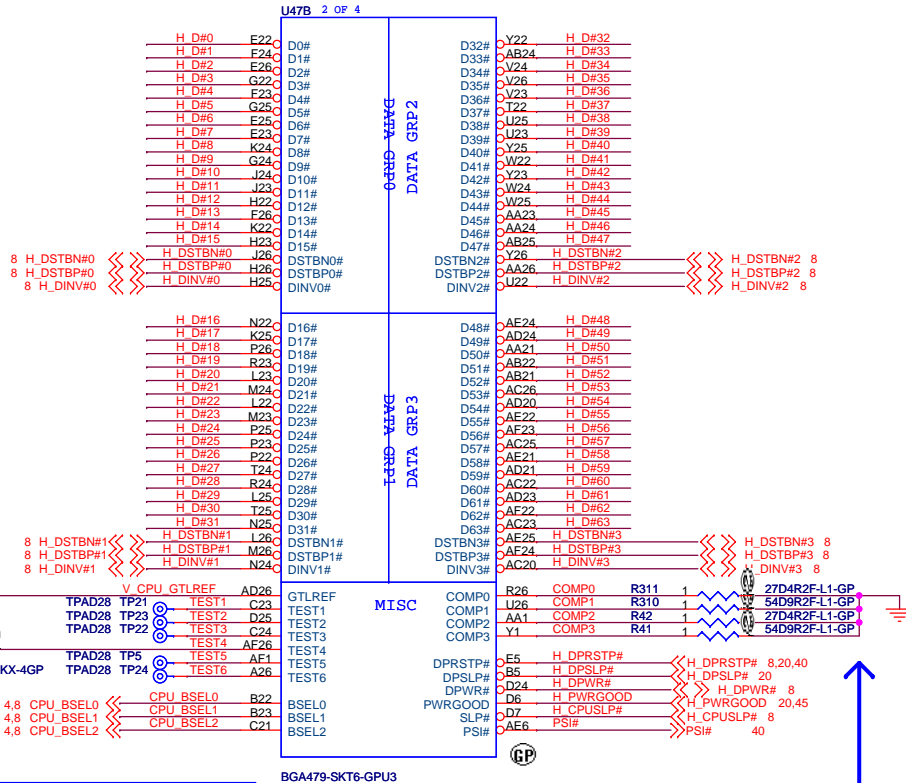
CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation



Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

<Core Design>

8 H_D#0[0.63] <<>>



8 H_DSTBN#0
8 H_DSTBP#0
8 H_DINV#0

8 H_DSTBN#1
8 H_DSTBP#1
8 H_DINV#1

4.8 CPU_BSEL0
4.8 CPU_BSEL1
4.8 CPU_BSEL2

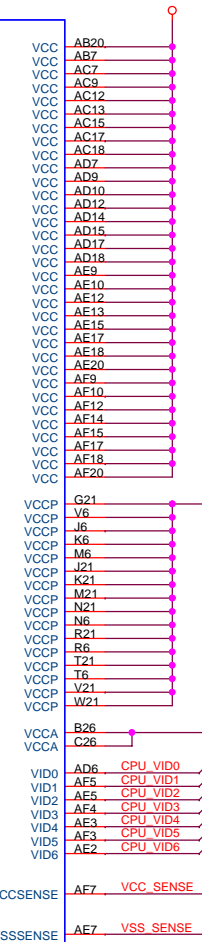
PLACE C617 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

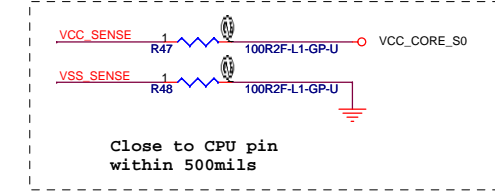
VCC_CORE_S0

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layout note:
place C618 near
PIN B26

Length match within
25 mils . The trace
width/space/other is
20/7/25 .



<Core Design>

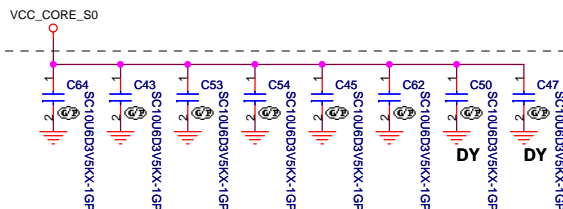
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Title			
Meron(2/3)-AGTL+-PWR			
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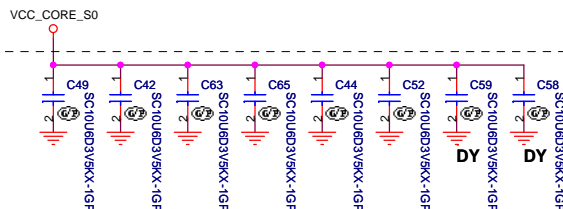
U47D 4 OF 4		
A4	VSS	P6
A8	VSS	P21
A11	VSS	P24
A14	VSS	R2
A16	VSS	R5
A19	VSS	R22
A23	VSS	R25
AF2	VSS	T1
B6	VSS	T4
B8	VSS	T23
B11	VSS	T26
B13	VSS	U3
B16	VSS	U6
B19	VSS	U21
B21	VSS	U24
B24	VSS	V2
C5	VSS	V5
C8	VSS	V22
C11	VSS	V25
C14	VSS	W1
C16	VSS	W4
C19	VSS	W23
C2	VSS	W26
C22	VSS	Y3
C25	VSS	Y6
D1	VSS	Y21
D4	VSS	Y24
D8	VSS	AA2
D11	VSS	AA5
D13	VSS	AA8
D16	VSS	AA11
D19	VSS	AA14
D23	VSS	AA16
D26	VSS	AA19
E3	VSS	AA22
E6	VSS	AA25
E8	VSS	AB1
E11	VSS	AB4
E14	VSS	AB8
E16	VSS	AB11
E19	VSS	AB13
E21	VSS	AB16
E24	VSS	AB19
F5	VSS	AB23
F8	VSS	AB26
F11	VSS	AC3
F13	VSS	AC6
F16	VSS	AC8
F19	VSS	AC11
F2	VSS	AC14
F22	VSS	AC16
F25	VSS	AC19
G4	VSS	AC21
G1	VSS	AC24
G23	VSS	AD2
G26	VSS	AD5
H3	VSS	AD8
H6	VSS	AD11
H21	VSS	AD13
H24	VSS	AD16
J2	VSS	AD19
J5	VSS	AD22
J22	VSS	AD25
J25	VSS	AE1
K1	VSS	AE4
K4	VSS	AE8
K23	VSS	AE11
K26	VSS	AE14
L3	VSS	AE16
L6	VSS	AE19
L21	VSS	AE23
L24	VSS	AE26
M2	VSS	A2
M5	VSS	AF6
M22	VSS	AF8
M25	VSS	AF11
N1	VSS	AF13
N4	VSS	AF16
N23	VSS	AF19
N26	VSS	AF21
P3	VSS	A25
	VSS	AF25

BGA479-SKT6-GPU3

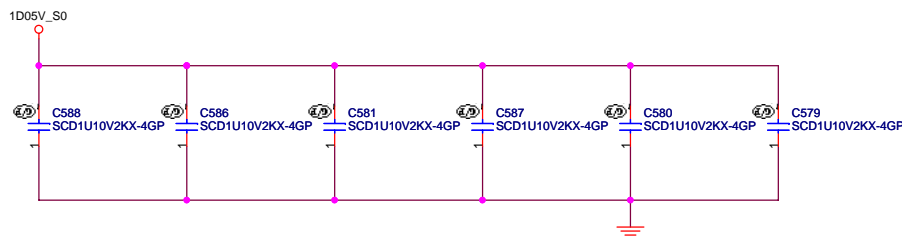
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequencd
Decoupling

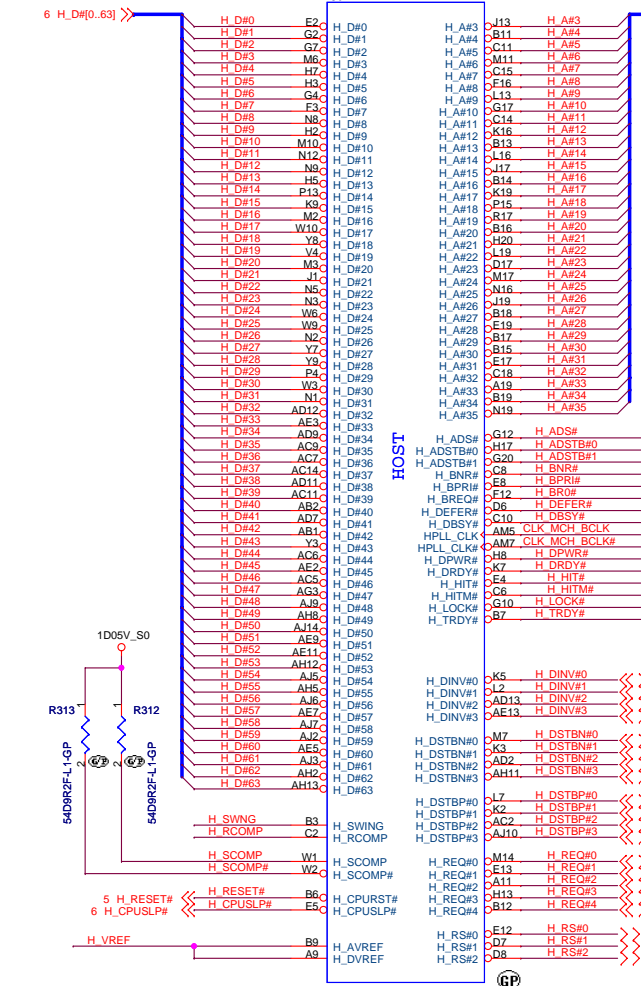


Place these
inside socket
cavity on L1
(North side
Secondary)

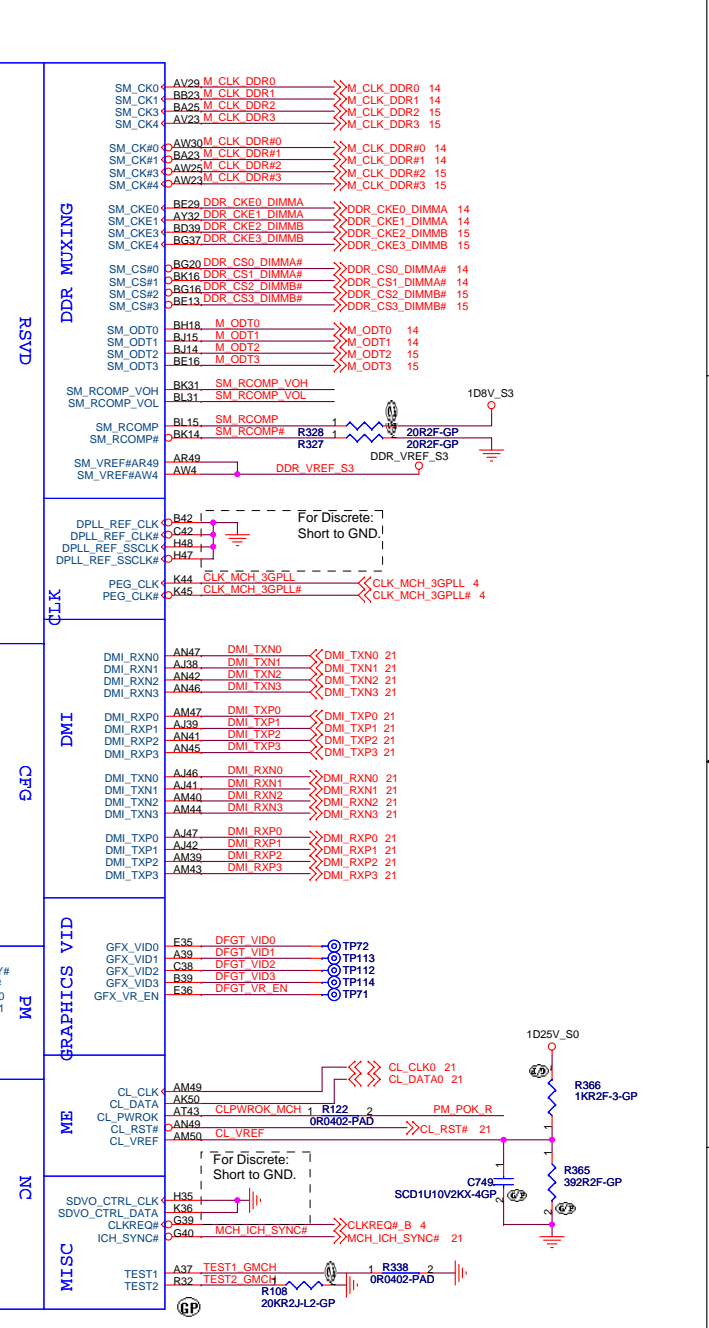
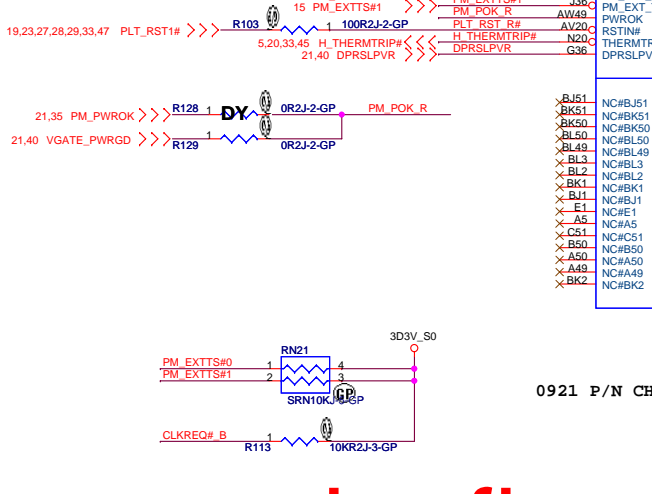
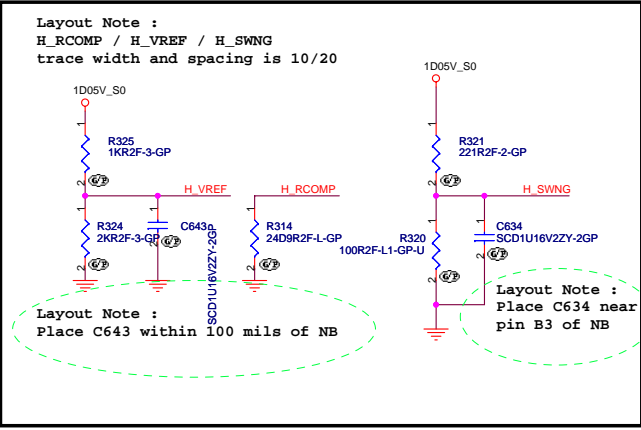
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Title		
Meron(3/3)-GND&Bypass		
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layout note :
Route H_SCOMP# and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



0921 P/N CHANGE TO 71.CREST.M02

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CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size Custom Document Number Hawke-Intel Rev -1

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<<>> DDR_A_D[0..63] 14
>>> DDR_A_BS[0..2] 14
>>> DDR_A_DM[0..7] 14
<<>> DDR_A_DQS[0..7] 14
<<>> DDR_A_DQS#[0..7] 14
>>> DDR_A_MA[0..14] 14

<<>> DDR_B_D[0..63] 15
>>> DDR_B_BS[0..2] 15
>>> DDR_B_DM[0..7] 15
<<>> DDR_B_DQS[0..7] 15
<<>> DDR_B_DQS#[0..7] 15
>>> DDR_B_MA[0..14] 15

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BE40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AV15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#
DDR A D50	AT5	SA_DQ50			
DDR A D51	AT7	SA_DQ51	SA_WE#	BA19	DDR A WE#
DDR A D52	AY6	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR5	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

DDR SYSTEM MEMORY A

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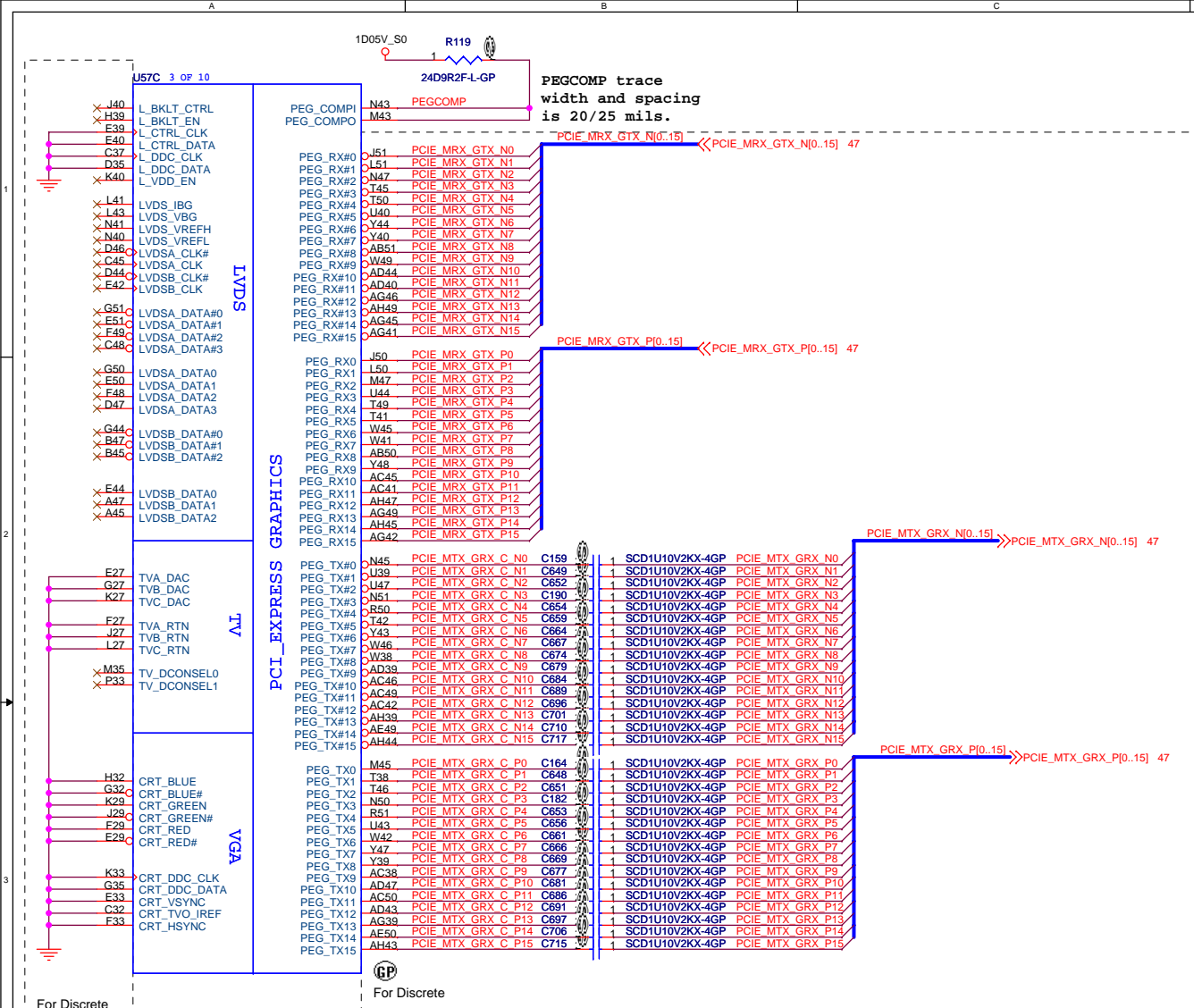
DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BE50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ44	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AI50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BE25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BL5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BK5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BE4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN#
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BJ2	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AJ2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

DDR SYSTEM MEMORY B

<Core Design>

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Title		CRESTLINE(2/6)-DDR2 A/B CH	
Size	Document Number	Hawke-Intel	
A3		-1	
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Strap Pin Table

CFG[2:0] FSB Freq select

CFG5 (DMI select)

CFG6

CFG7 (CPU Strap)

CFG8 (Low power PCIE)

CFG9 (PCIE Graphics Lane Reversal)

CFG[11:10]

CFG[13:12] (XOR/ALLZ)

CFG[15:14]

CFG16 (FSB Dynamic ODT)

CFG[18:17]

SDVO_CTRLDATA

CFG19(DMI Lane Reversal)

CFG20(PCIE/SDVO consurrent)

010 = FSB 800MHz
011 = FSB 667MHz
Others = Reserved

0 = DMI x 2
1 = DMI x 4 *

Reserved

0 = Reserved
1 = Mobile CPU *

0 = Normal mode
1 = Low Power mode *

0 = Reverse Lane
1 = Normal Operation *

Reserved

00 = Reserved
01 = XOR Mode Enabled
10 = All Z Mode Enabled
11 = Normal Operation (Default)*

Reserved

0 = Disable
1 = Enable *

Reversed

0 = No SDVO Device Present *
1 = SDVO Device Present

0 = Normal Operation
(Lane number in Order) *
1 = Reverse lane

0 = Only PCIE or SDVO is operational *
1 = PCIE/SDVO are operating simu.

<Core Design>

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Title		CRESTLINE(3/6)-VGA/LVDS/TV	
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A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AD1	VSS	VSS	B30
AD21	VSS	VSS	B35
AD26	VSS	VSS	B38
AD29	VSS	VSS	B43
AD3	VSS	VSS	B46
AD41	VSS	VSS	B5
AD45	VSS	VSS	B8
AD49	VSS	VSS	BA1
AD5	VSS	VSS	BA17
AD50	VSS	VSS	BA18
AD8	VSS	VSS	BA2
AE10	VSS	VSS	BA24
AE14	VSS	VSS	BB12
AE6	VSS	VSS	BB25
AF20	VSS	VSS	BB40
AF23	VSS	VSS	BB44
AF24	VSS	VSS	BB49
AF31	VSS	VSS	BB8
AG2	VSS	VSS	BC16
AG38	VSS	VSS	BC24
AG43	VSS	VSS	BC25
AG47	VSS	VSS	BC36
AG50	VSS	VSS	BC40
AH3	VSS	VSS	BC51
AH40	VSS	VSS	BD13
AH41	VSS	VSS	BD2
AH7	VSS	VSS	BD28
AH9	VSS	VSS	BD45
AJ11	VSS	VSS	BD48
AJ13	VSS	VSS	BD5
AJ21	VSS	VSS	BE1
AJ24	VSS	VSS	BE19
AJ29	VSS	VSS	BE23
AJ32	VSS	VSS	BE30
AJ43	VSS	VSS	BE42
AJ45	VSS	VSS	BE51
AJ49	VSS	VSS	BE8
AK20	VSS	VSS	BF12
AK21	VSS	VSS	BF16
AK26	VSS	VSS	BF36
AK28	VSS	VSS	BG19
AK31	VSS	VSS	BG2
AK51	VSS	VSS	BG24
AL1	VSS	VSS	BG29
AM11	VSS	VSS	BG39
AM13	VSS	VSS	BG48
AM3	VSS	VSS	BG5
AM4	VSS	VSS	BG51
AM41	VSS	VSS	BH17
AM45	VSS	VSS	BH30
AN1	VSS	VSS	BH44
AN38	VSS	VSS	BH46
AN39	VSS	VSS	BH8
AN43	VSS	VSS	BJ11
AN5	VSS	VSS	BJ13
AN7	VSS	VSS	BJ38
AP4	VSS	VSS	BJ4
AP48	VSS	VSS	BJ42
AP50	VSS	VSS	BJ46
AR11	VSS	VSS	BK12
AR2	VSS	VSS	BK17
AR39	VSS	VSS	BK25
AR44	VSS	VSS	BK29
AR47	VSS	VSS	BK36
AT10	VSS	VSS	BK40
AT14	VSS	VSS	BK44
AT41	VSS	VSS	BK6
AT49	VSS	VSS	BK8
AU1	VSS	VSS	BL11
AU23	VSS	VSS	BL13
AU29	VSS	VSS	BL19
AU3	VSS	VSS	BL22
AU36	VSS	VSS	BL37
AU49	VSS	VSS	BL47
AU51	VSS	VSS	C12
AV39	VSS	VSS	C16
AV48	VSS	VSS	C19
AW1	VSS	VSS	C28
AW12	VSS	VSS	C29
AW16	VSS	VSS	C33
		VSS	C36
		VSS	C41

VSS

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C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E28	VSS	VSS	Y11
E32	VSS	VSS	P29
E47	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS		
F50	VSS		
G1	VSS		
G13	VSS		
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	HS0
G48	VSS		
G8	VSS		
H24	VSS		
H28	VSS		
H4	VSS		
H45	VSS		
J11	VSS		
J16	VSS		
J2	VSS		
J24	VSS		
J28	VSS		
J33	VSS		
J35	VSS		
J39	VSS		
K12	VSS		
K47	VSS		
K8	VSS		
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N39	VSS		
N44	VSS		
N49	VSS		
N7	VSS		
P19	VSS		
P2	VSS		
P23	VSS		
P3	VSS		
P50	VSS		
R49	VSS		
T39	VSS		
T43	VSS		
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U41	VSS		
U45	VSS		
U50	VSS		
V2	VSS		
V3	VSS		

VSS

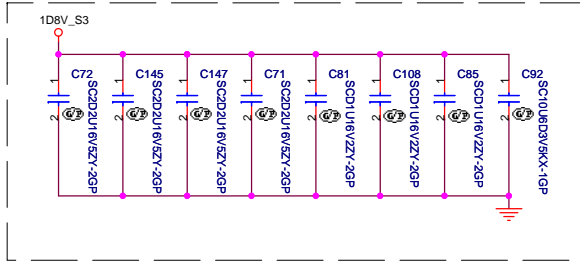
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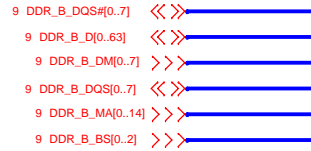
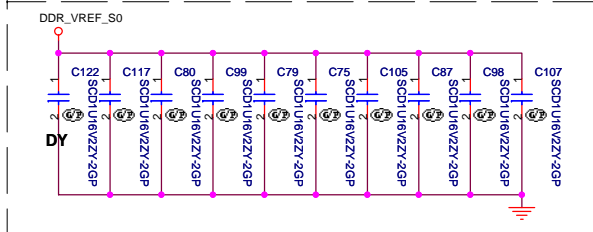
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Size	Document Number	Hawke-Intel	
A3		Rev -1	
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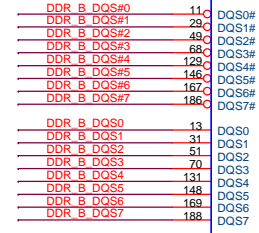
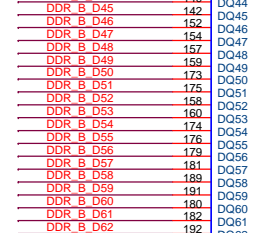
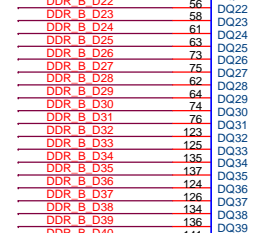
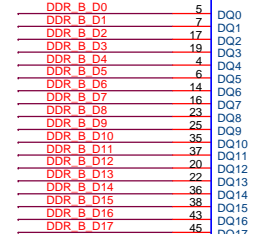
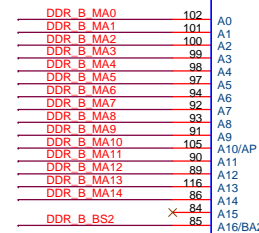
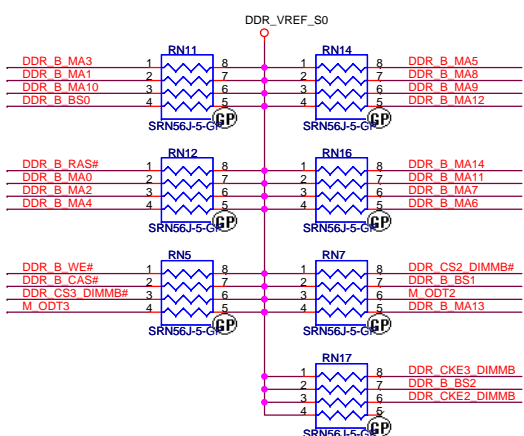
Layout Note:
Place near DM2



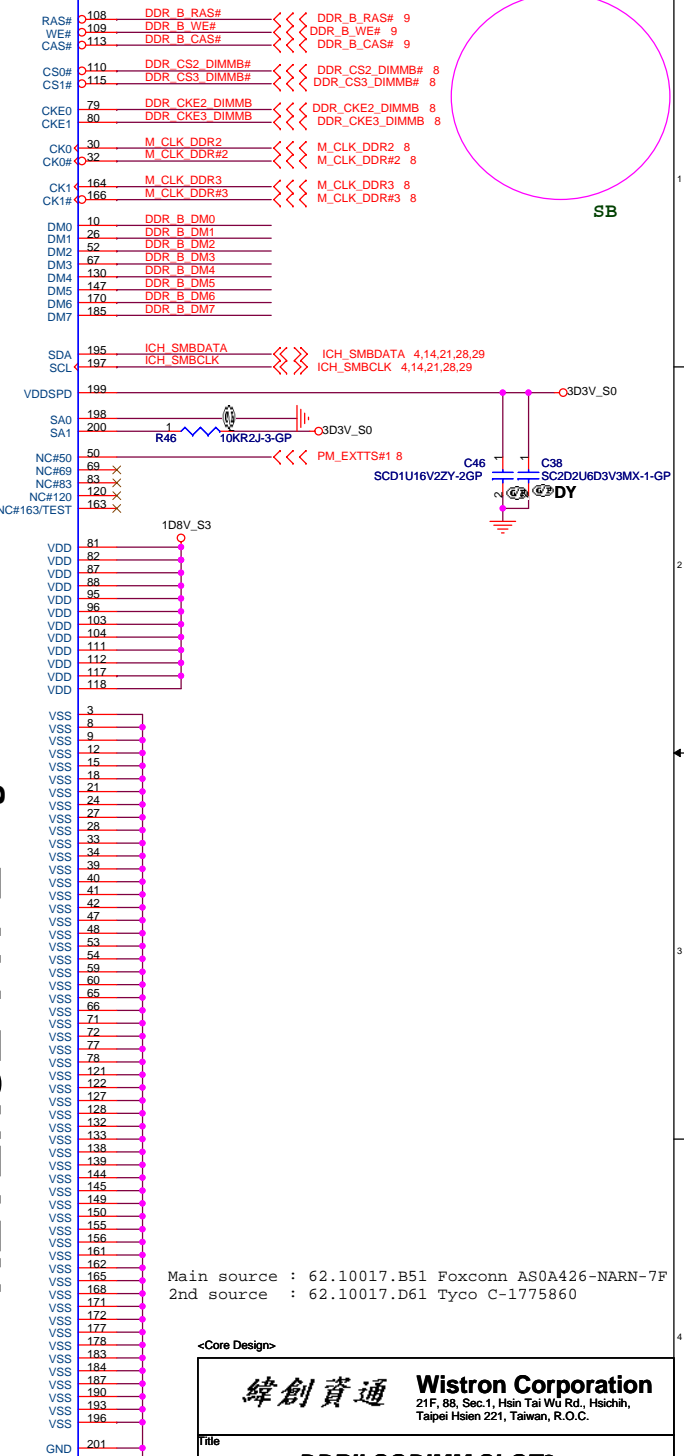
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"



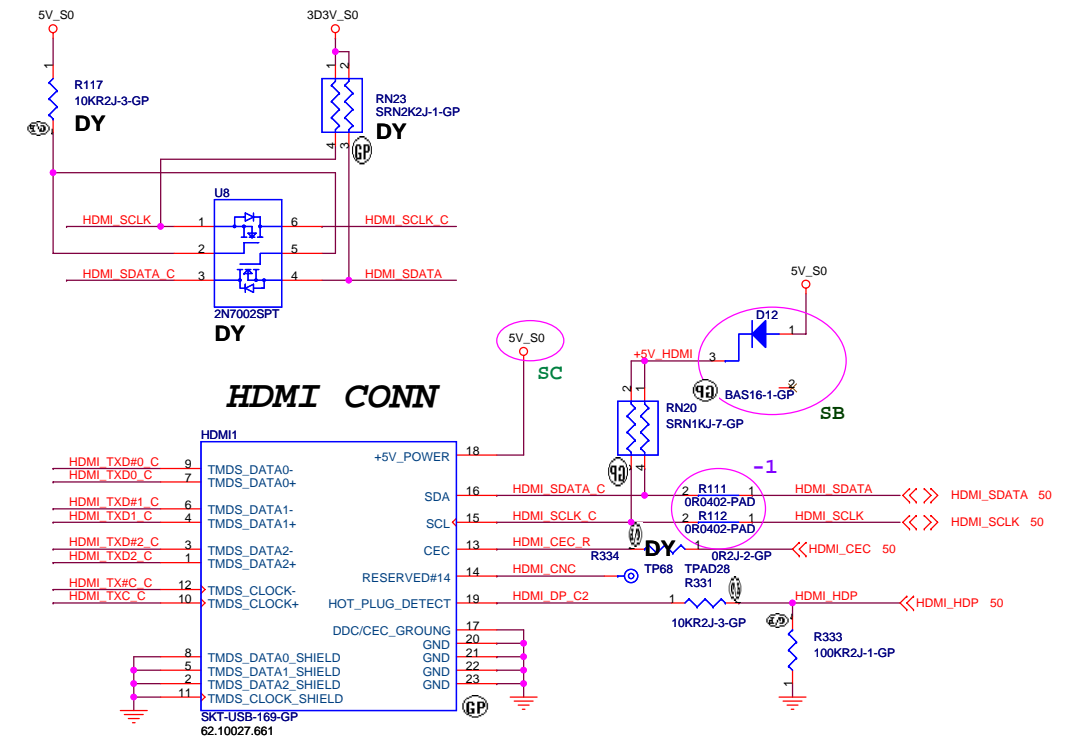
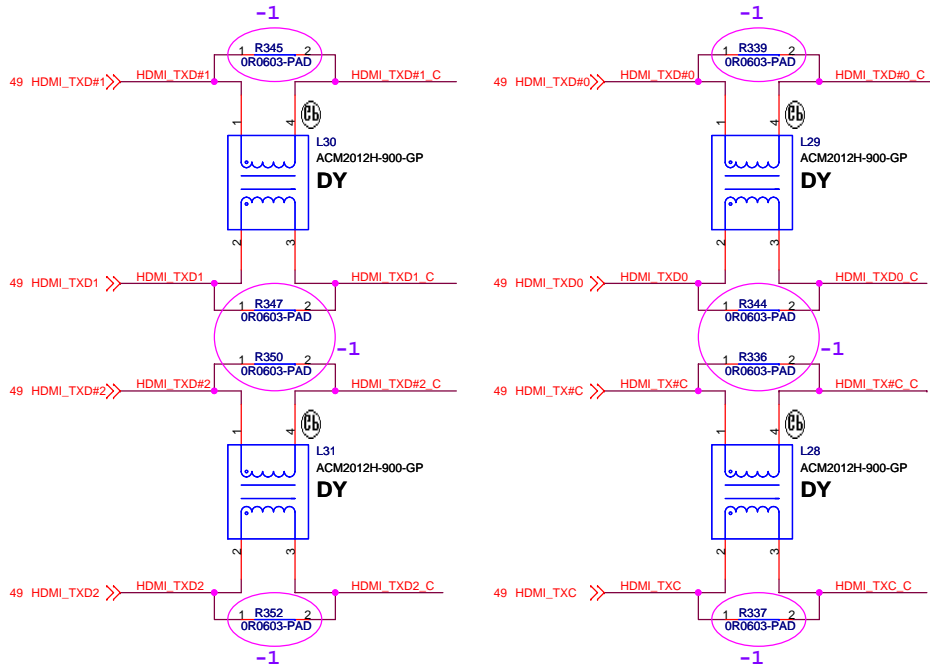
REVERSE TYPE High 9.2 mm



Main source : 62.10017.B51 Foxconn AS0A426-NARN-7F
2nd source : 62.10017.D61 Tyco C-1775860

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>DDRII-SODIMM SLOT2</p>	
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<p>Size</p>	<p>Hawke-Intel</p>
<p>Custom</p>	<p>Rev -1</p>
<p>Date: Sunday, September 09, 2007</p>	<p>Sheet 15 of 57</p>

HDMI I/F & CONNECTOR

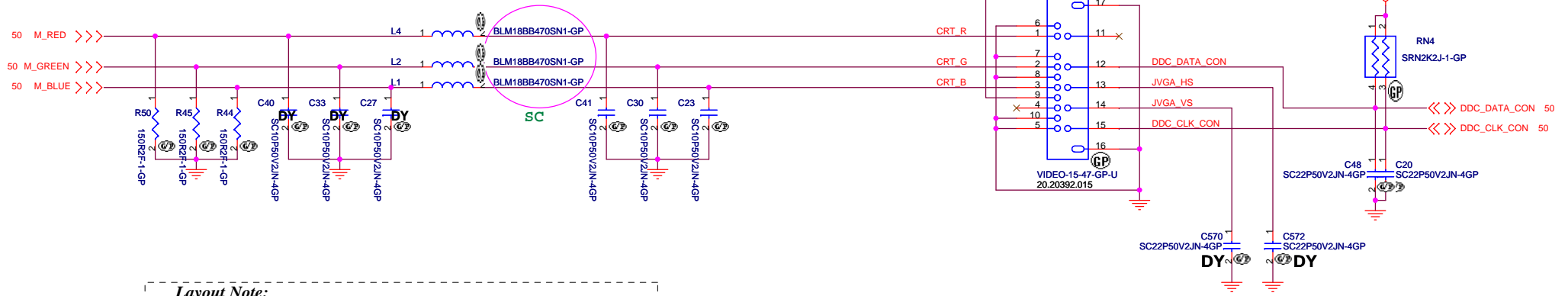


Main source : 62.10027.661 Molex 47408-0201
2nd source : 62.10078.121 Tyco C1759548-1

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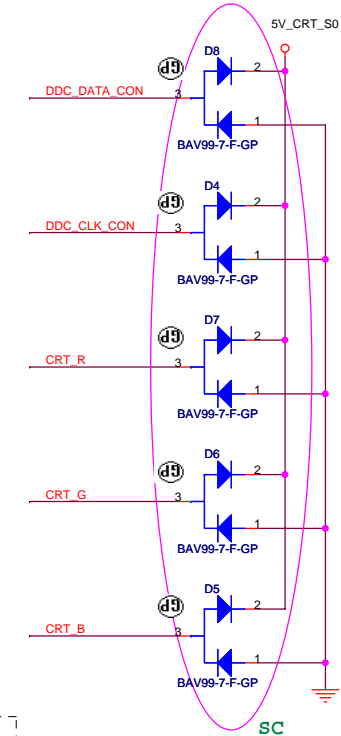
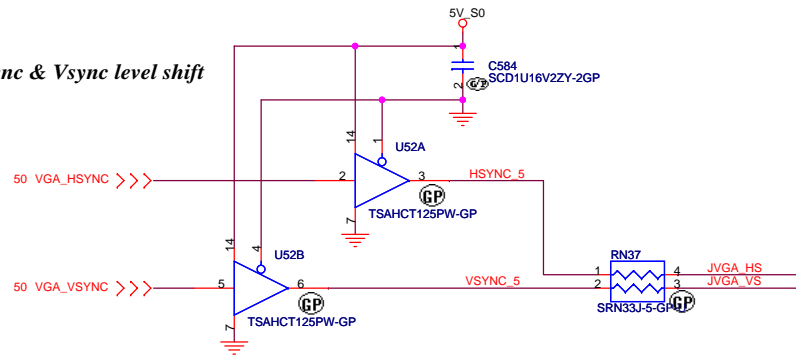
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Title	HDMI
Size A3	Document Number Hawke-Intel
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CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



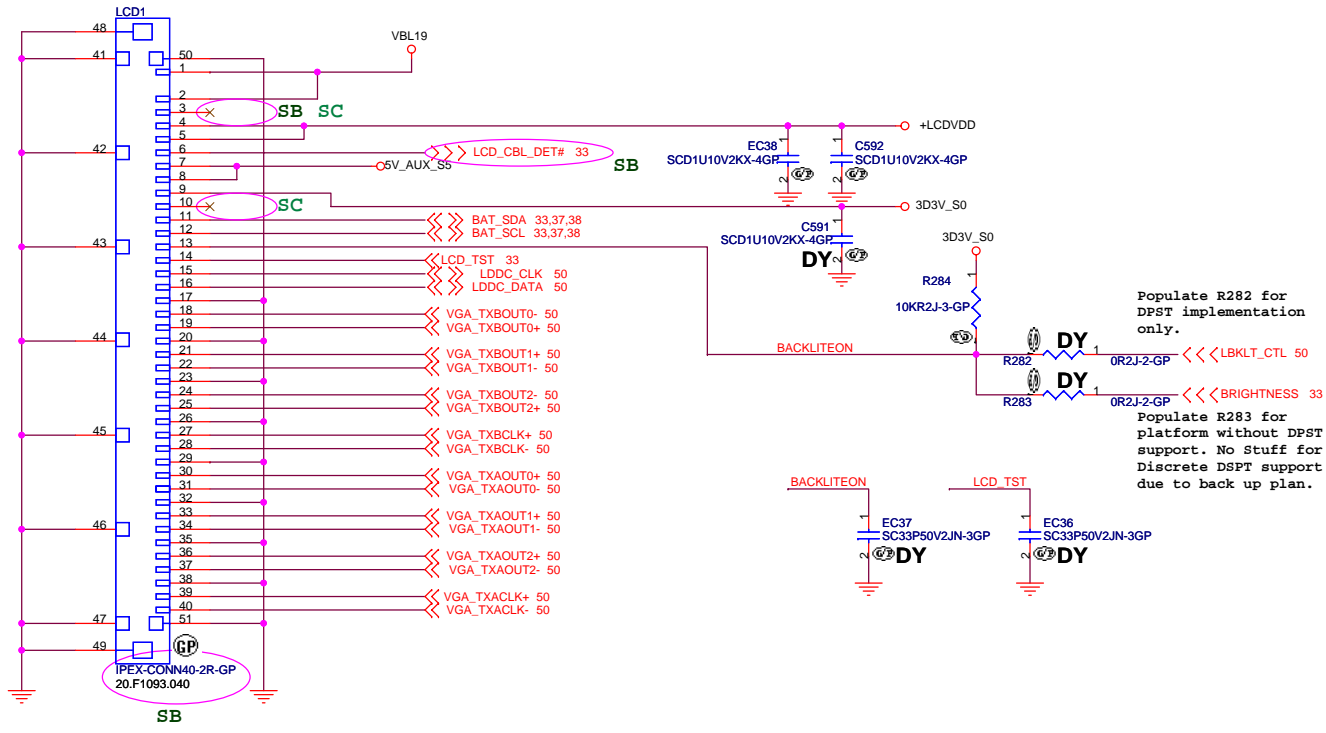
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TP28-75-GP	TP176	DDC_DATA_CON
TP28-75-GP	TP179	DDC_CLK_CON
TP28-75-GP	TP178	CRT_R
TP28-75-GP	TP180	CRT_G
TP28-75-GP	TP182	CRT_B
TP28-75-GP	TP181	JVGA_HS
TP28-75-GP	TP183	JVGA_VS

For AFTE, place them on the same side.

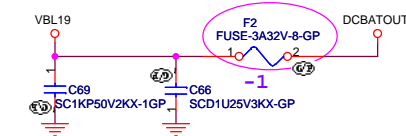
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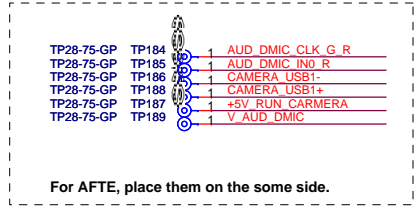
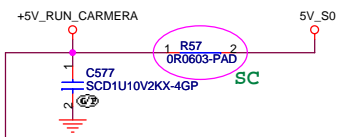
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Size A3	Document Number	Rev -1
Date: Sunday, September 09, 2007	Sheet 17 of 57	



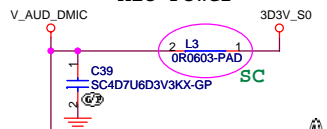
INVERTER POWER



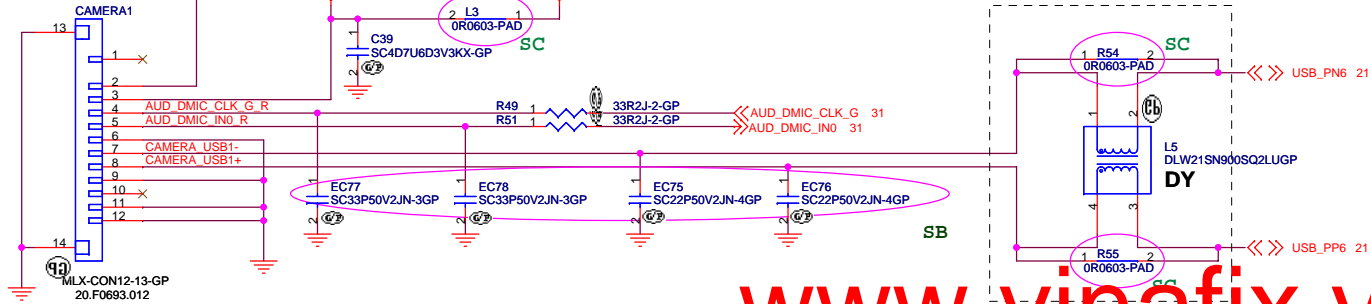
CAMERA Power



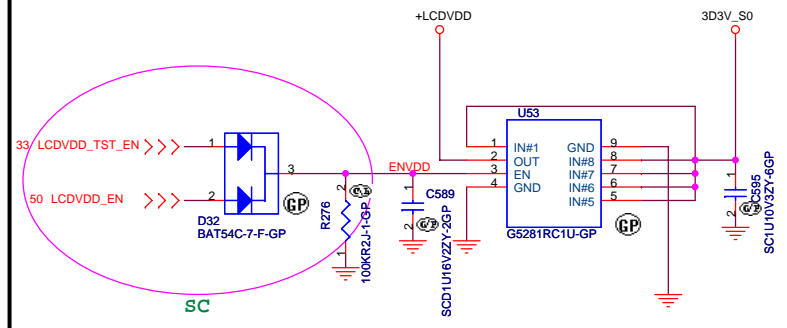
Mic Power



Place near connector CAMERA1.



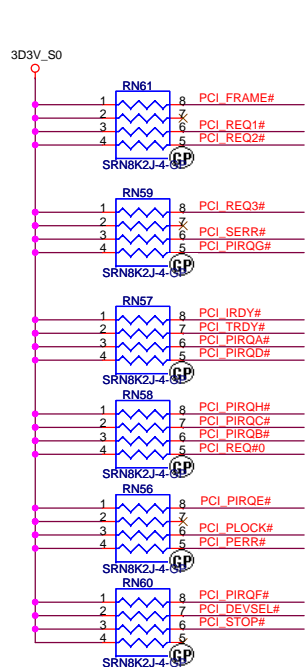
LCD POWER



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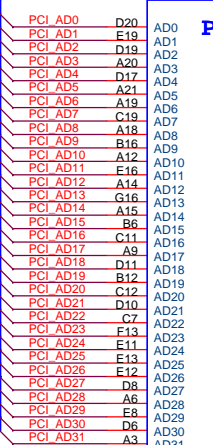
緯創資通 Wistron Corporation
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Title			LCD/Inverter/Camera		
Size	Document Number				Rev
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24 PCI_AD[0..31] <<> PCI_AD[0..31]

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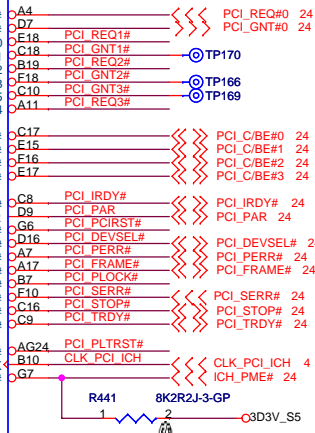
PCI

REQ0# GNT0#
REQ1#/GPIO50 GNT1#/GPIO51
REQ2#/GPIO52 GNT2#/GPIO53
REQ3#/GPIO54 GNT3#/GPIO55

C/BE0# C/BE1# C/BE2# C/BE3#
IRDY# PAR
PCIRST# DEVSEL#
PERR# FRAME#
PLOCK# SERR#
STOP# TRDY#
PLTRST#
PCICLK#
PME#

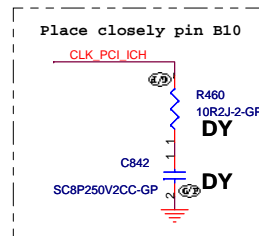
Interrupt I/F

PIRQA# PIRQB# PIRQC# PIRQD#
PIRQA#/GPIO2 PIRQB#/GPIO3
PIRQC#/GPIO4 PIRQD#/GPIO5



PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

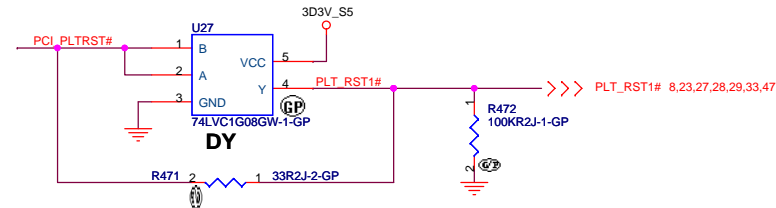
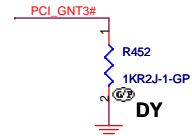


0504 P/N CHANGE TO 71.ICH8M.COU

ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

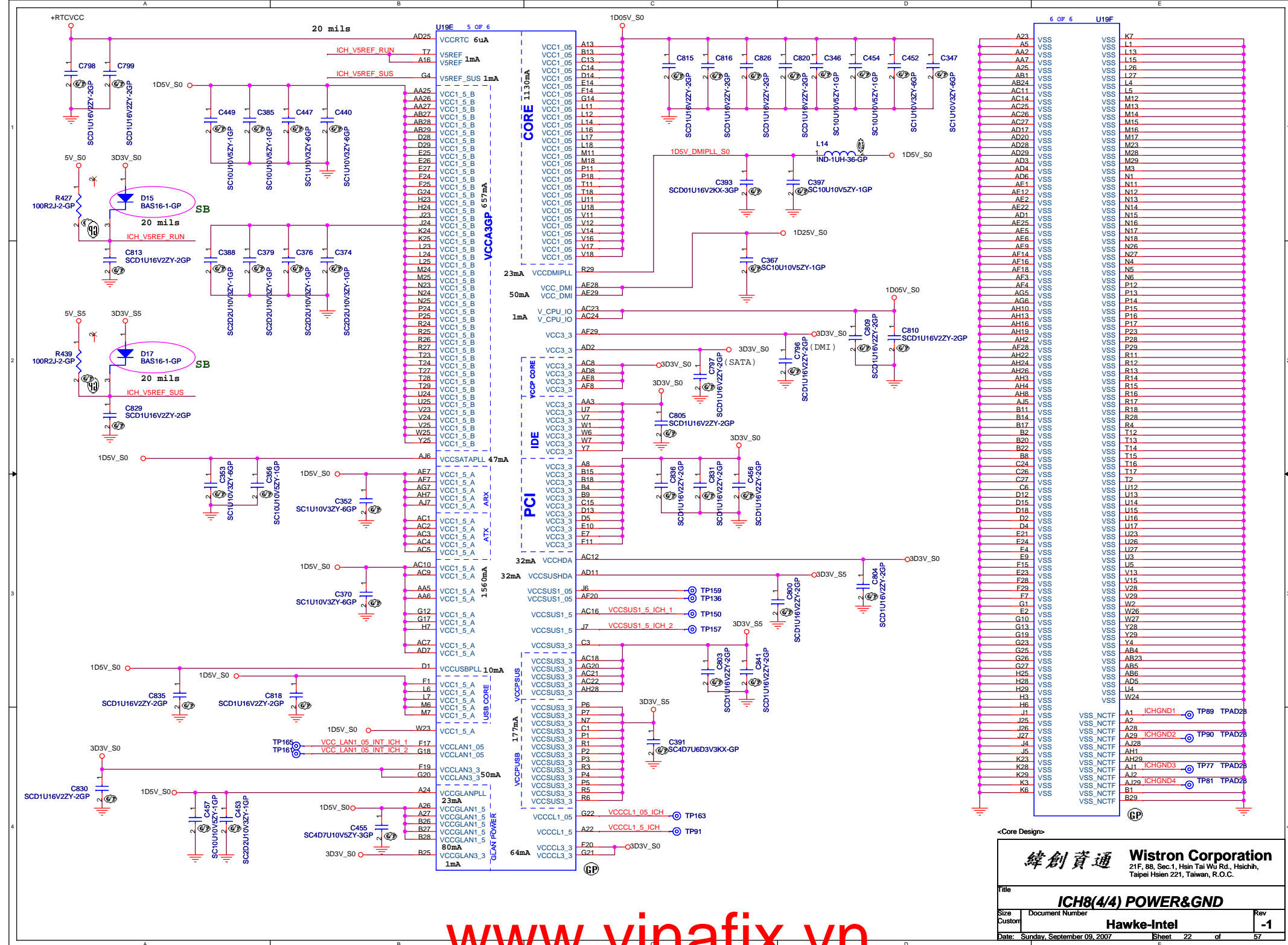


<Core Design>

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Title	ICH8(1/4)-PCI/INT		
Size A3	Document Number	Hawke-Intel	Rev -1
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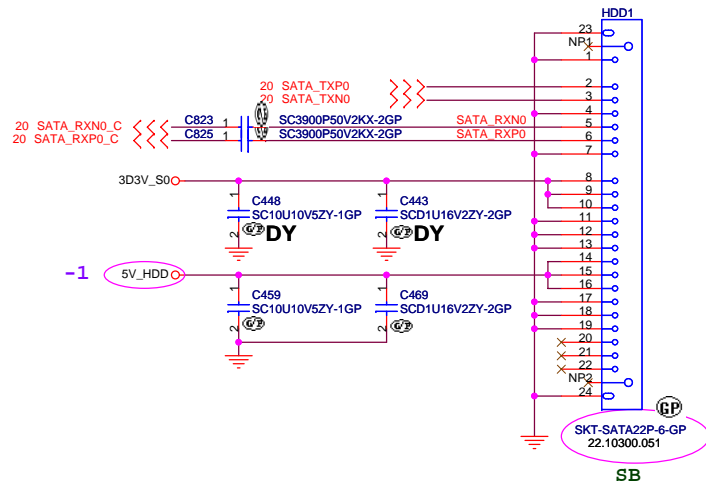
ICH8(4/4) POWER&GND

File: _____
Size: _____
Custom: _____
Date: Sunday, September 09, 2007
Sheet: 22 of 57

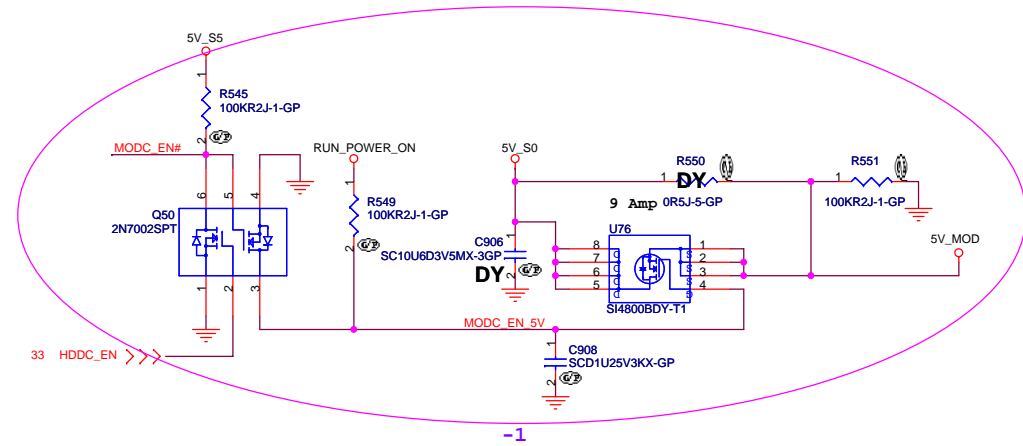
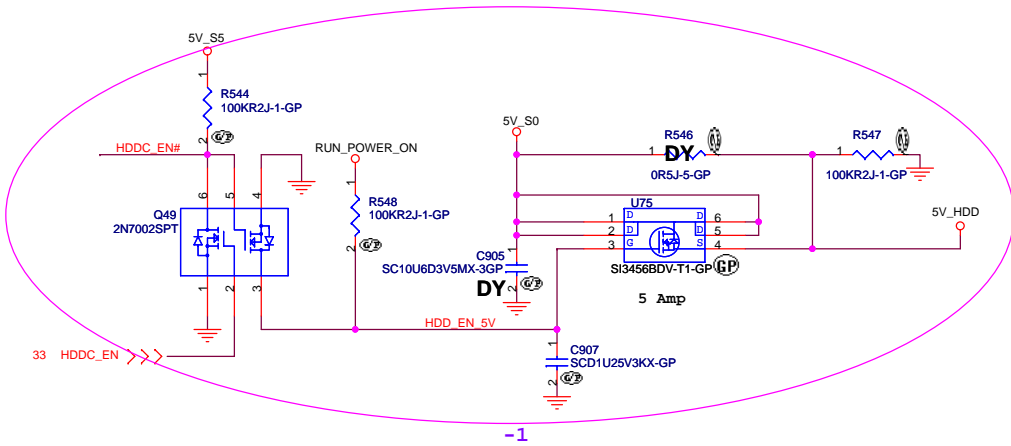
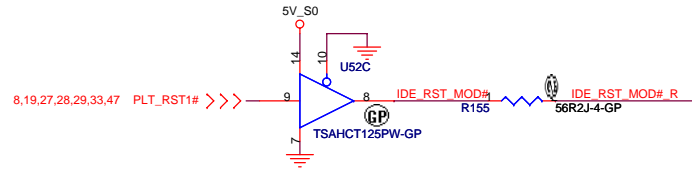
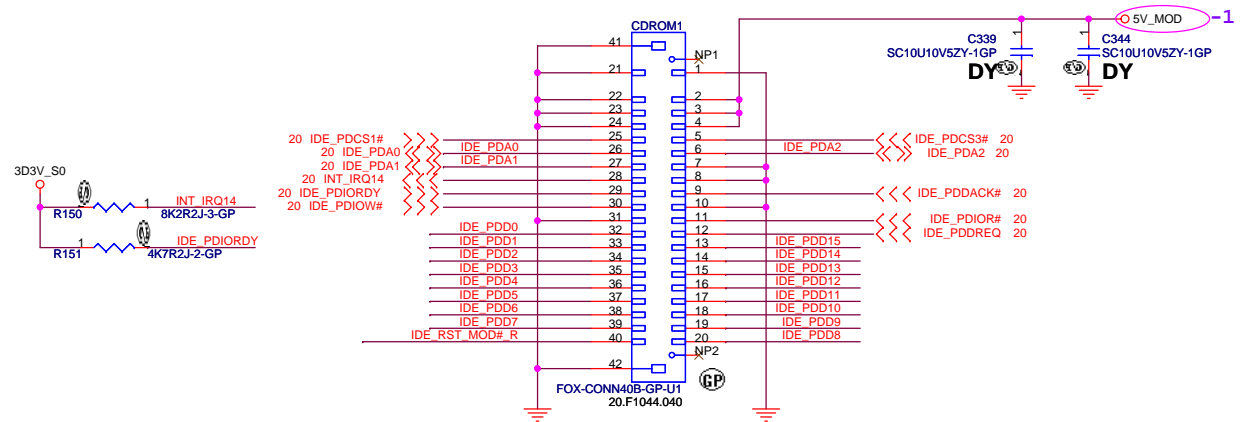
Hawke-Intel
Rev: -1

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SATA HDD Connector



ODD Connector

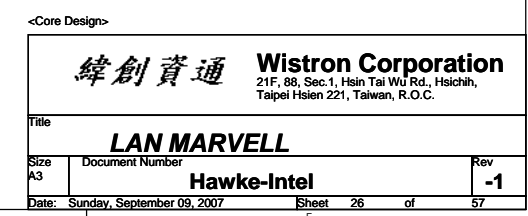


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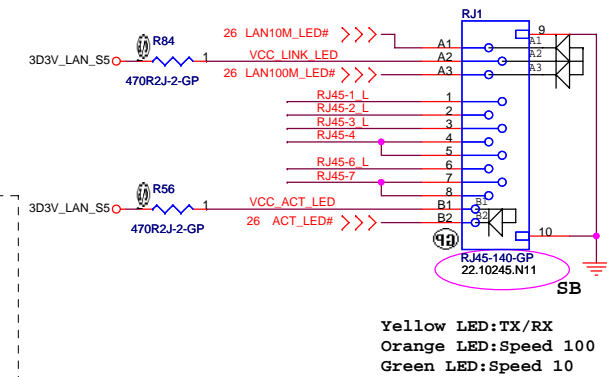
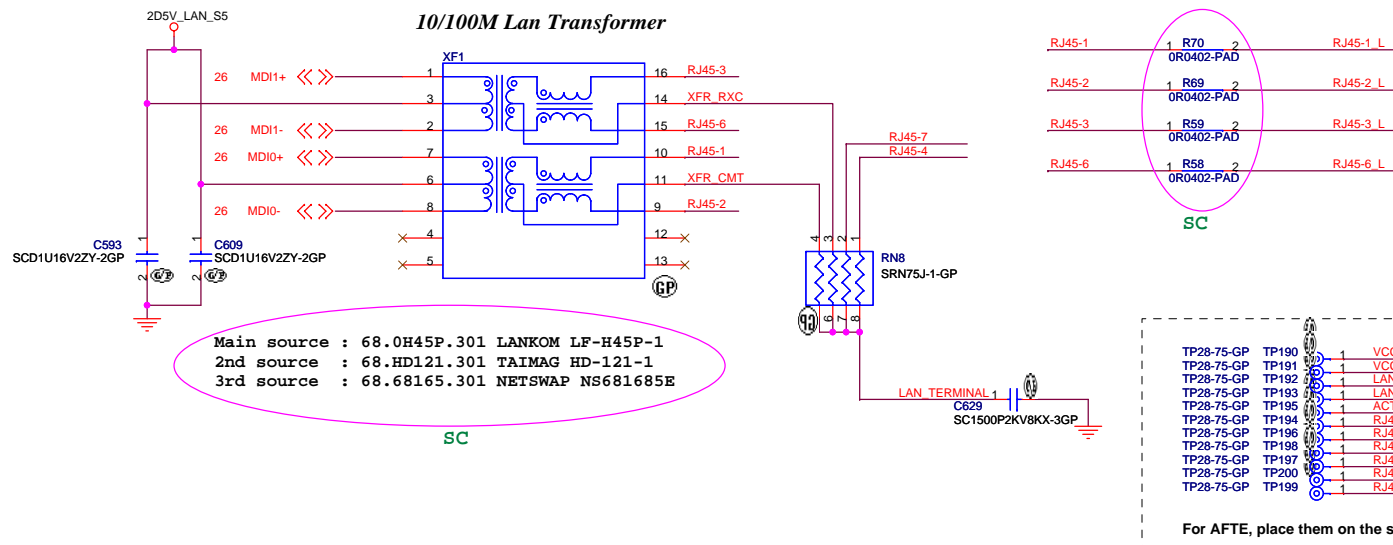
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Size A3	Document Number	Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007	Sheet 23	of 57	

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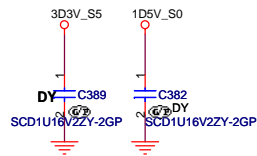
RJ45 Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

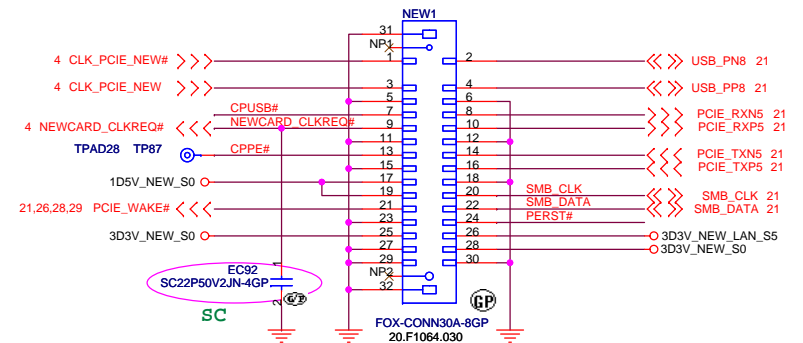
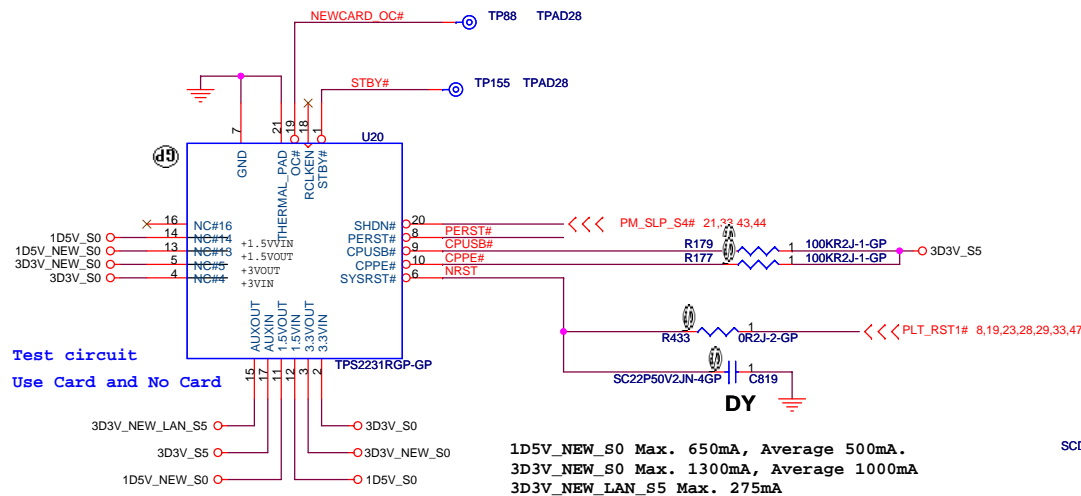
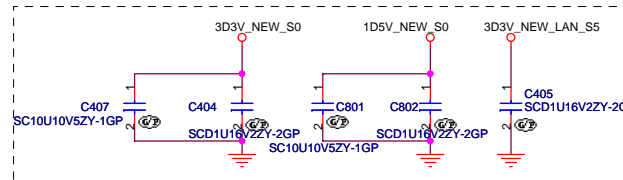


NEWCARD Connector

Place them Near to Chip



Place them Near to Connector

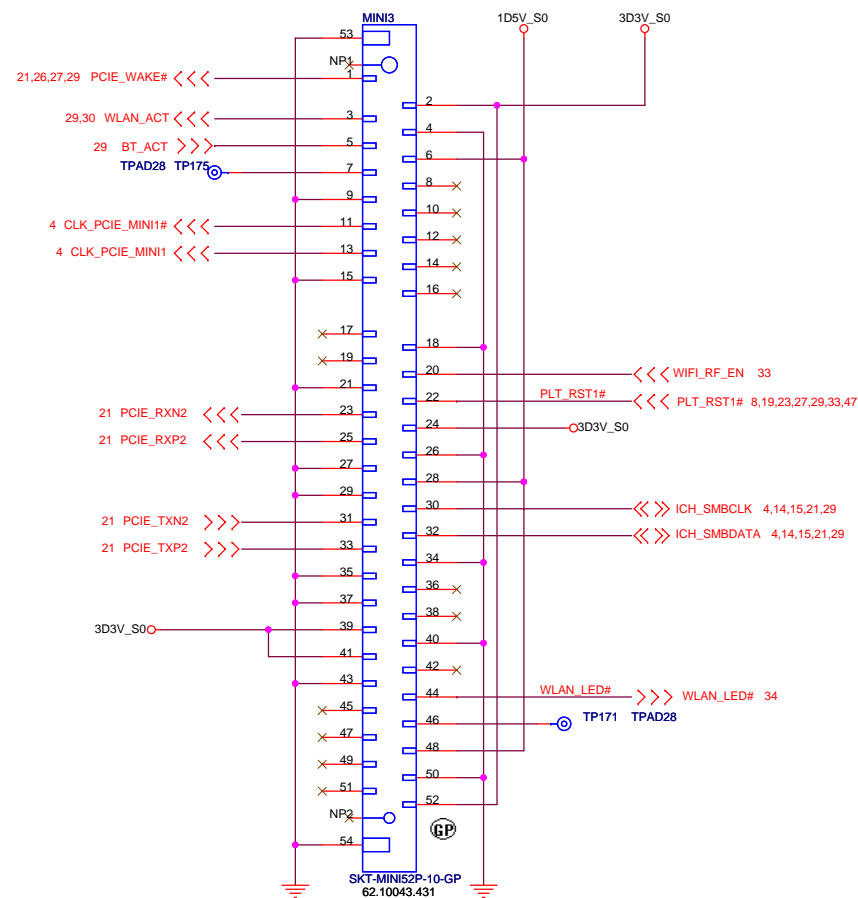


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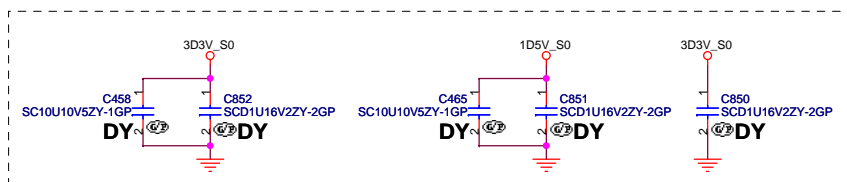
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Title		
LAN connector/NEW CARD		
Size A3	Document Number	Rev
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Mini Card Connector 1(802.11a/b/g)



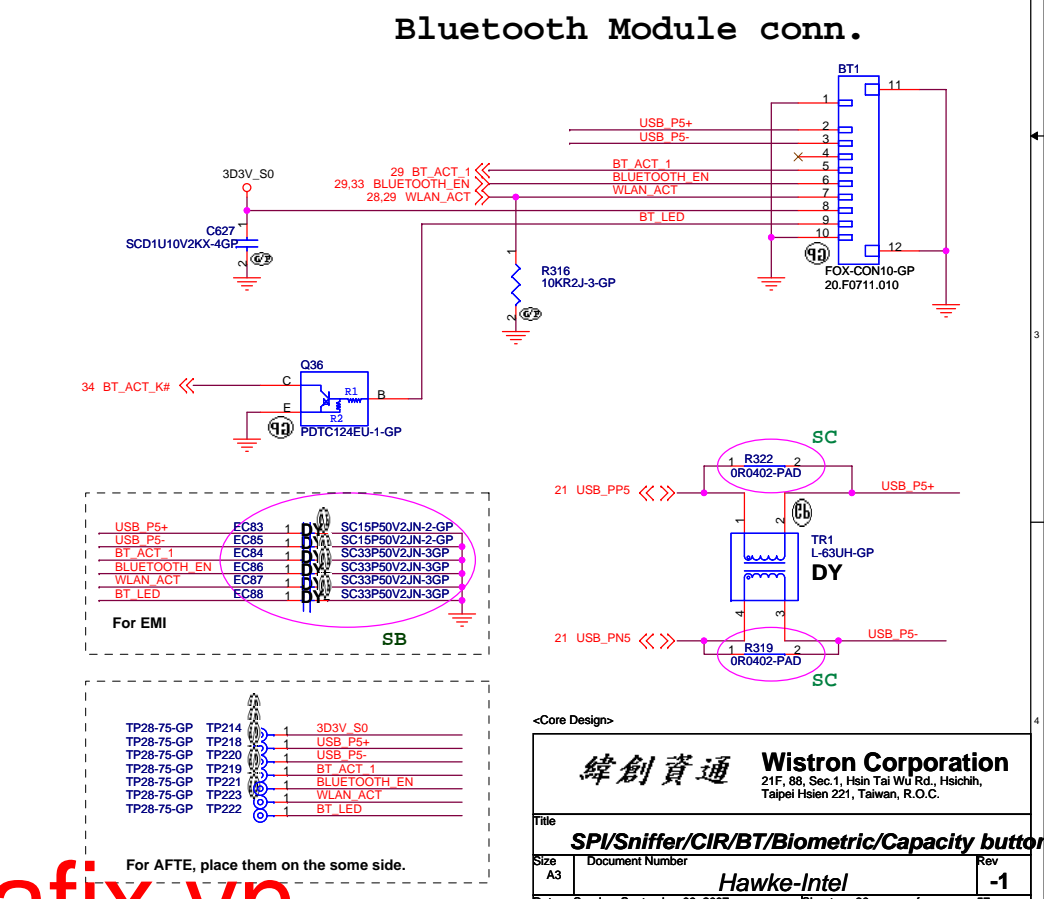
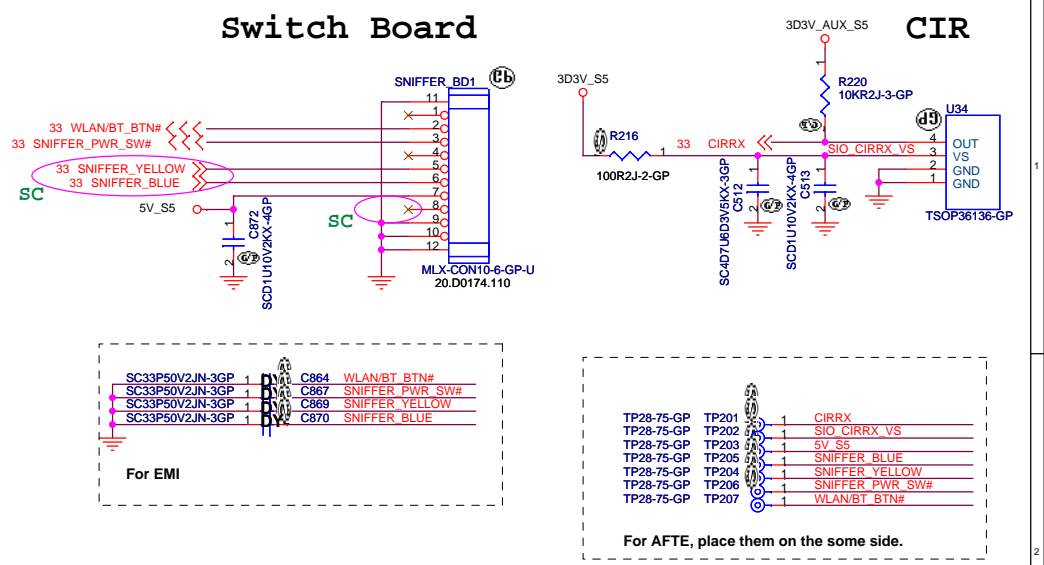
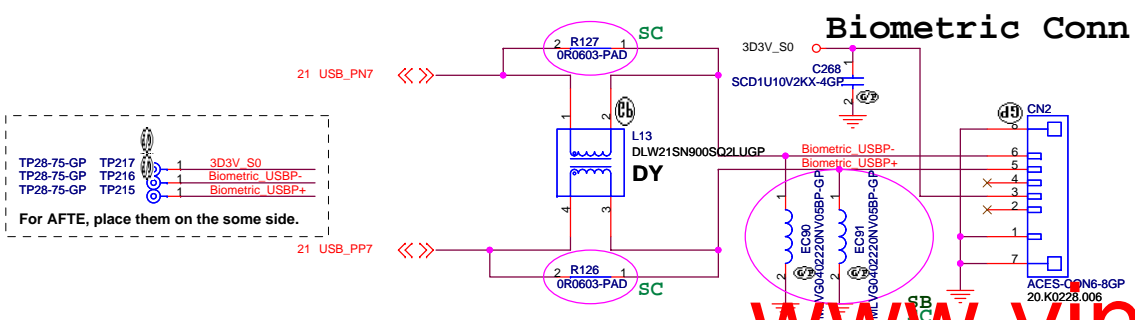
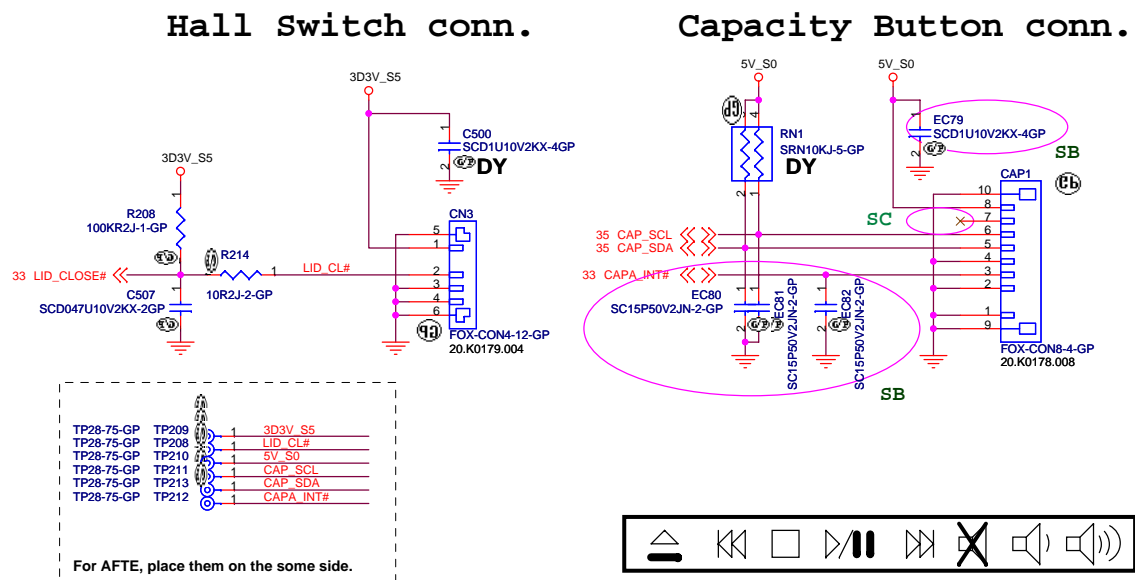
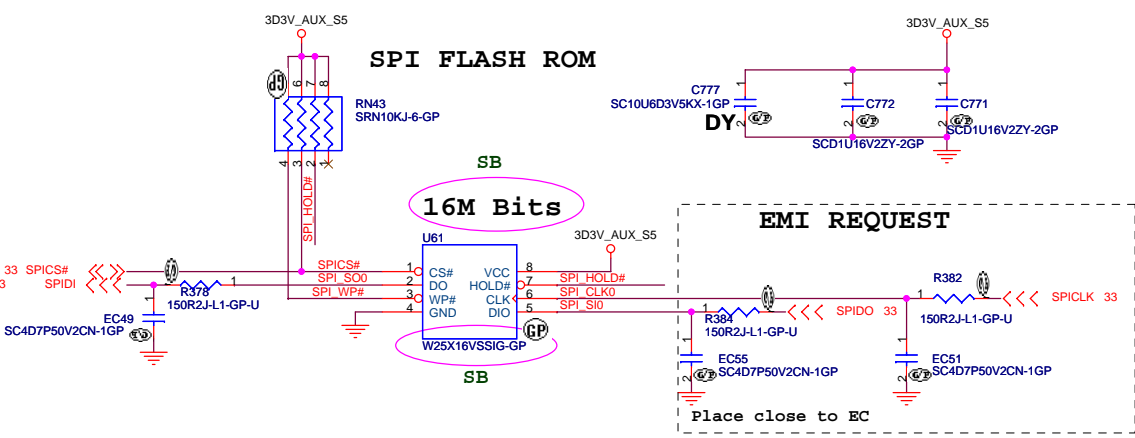
Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1

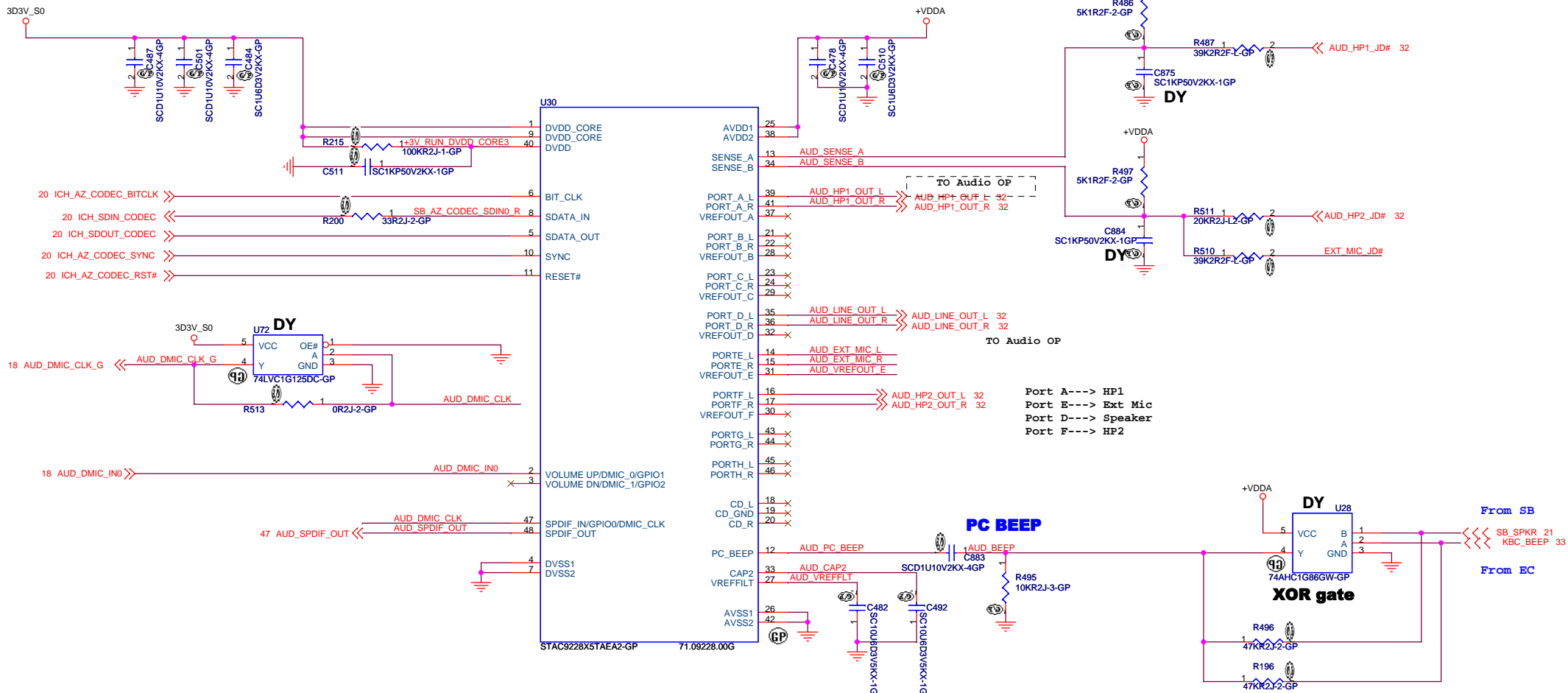


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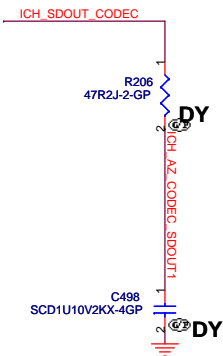
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Title		
MINI CARD CONN 1		
Size	Document Number	Rev
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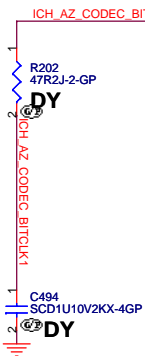




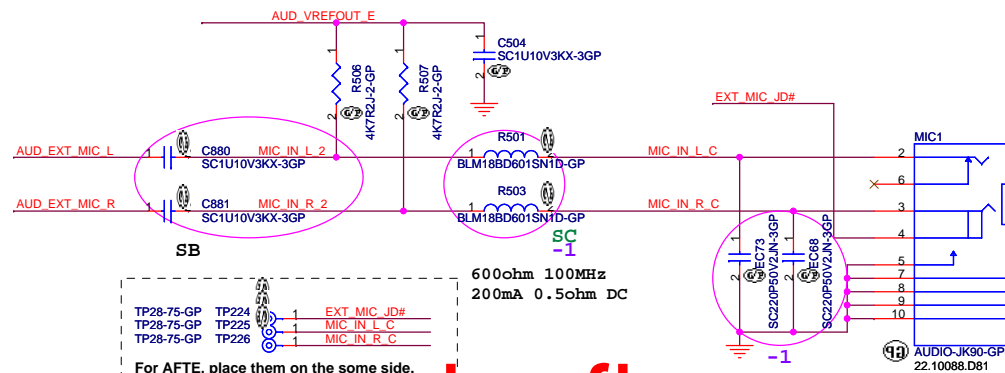
Azalia I/F EMI



Azalia I/F EMI



MIC IN



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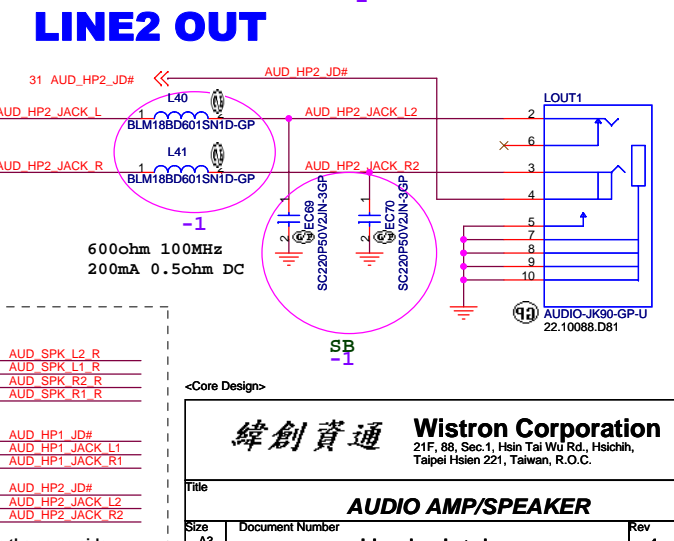
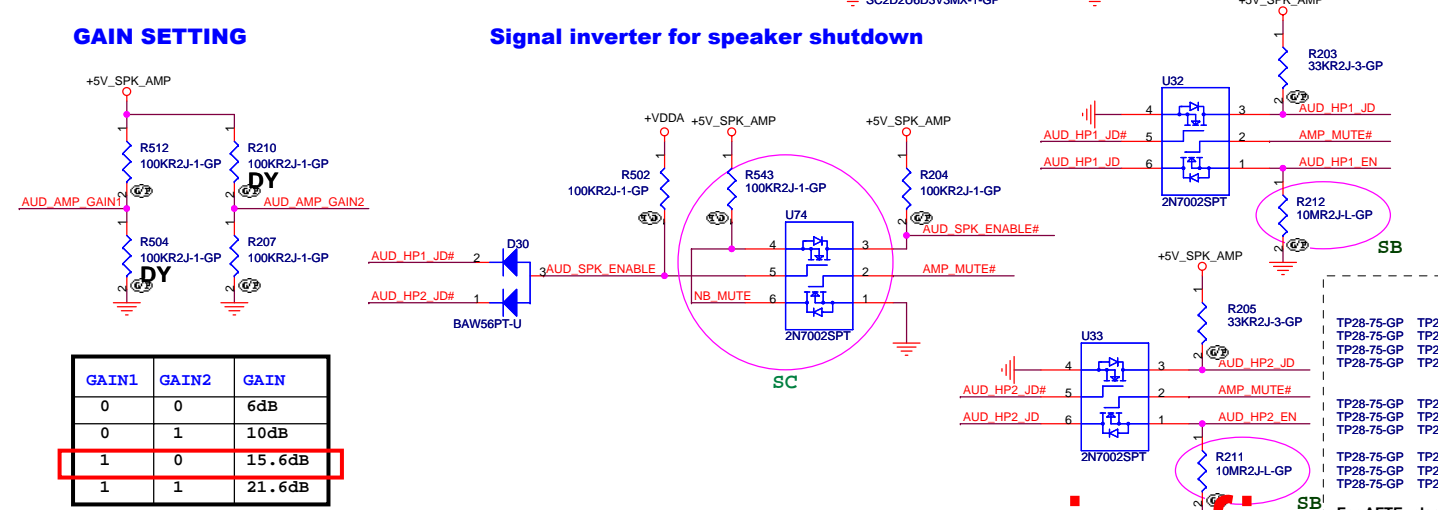
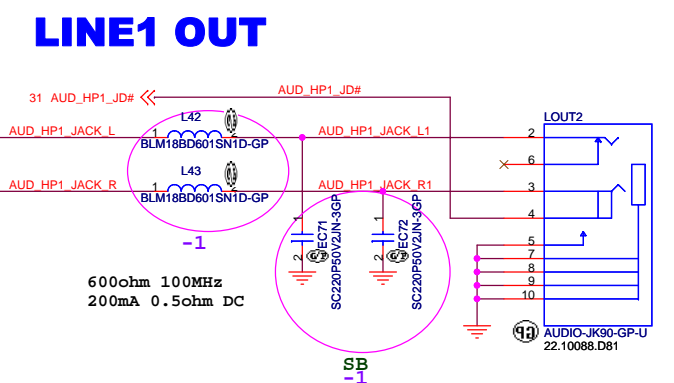
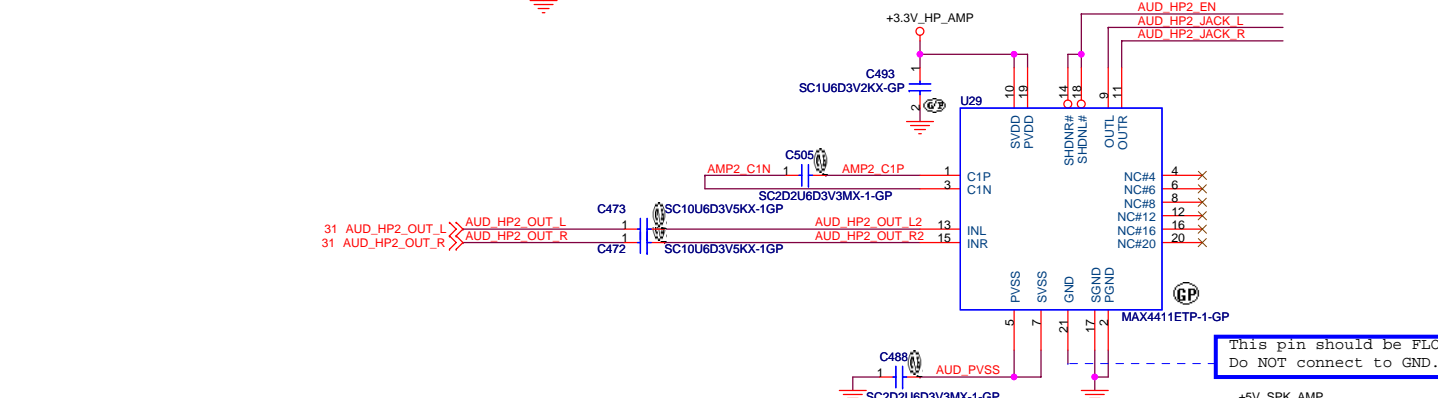
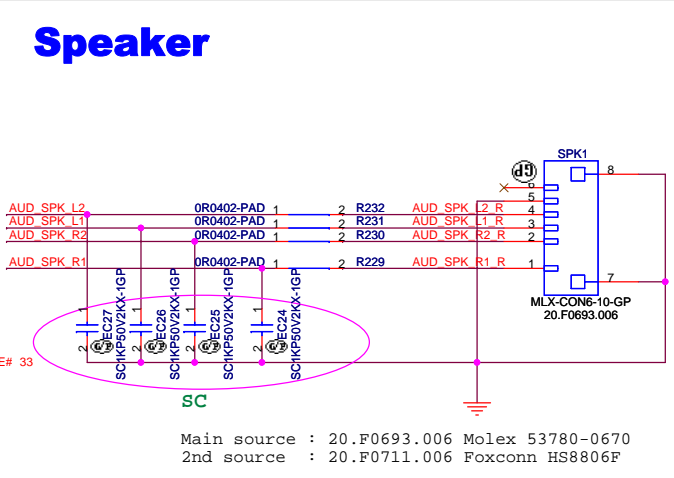
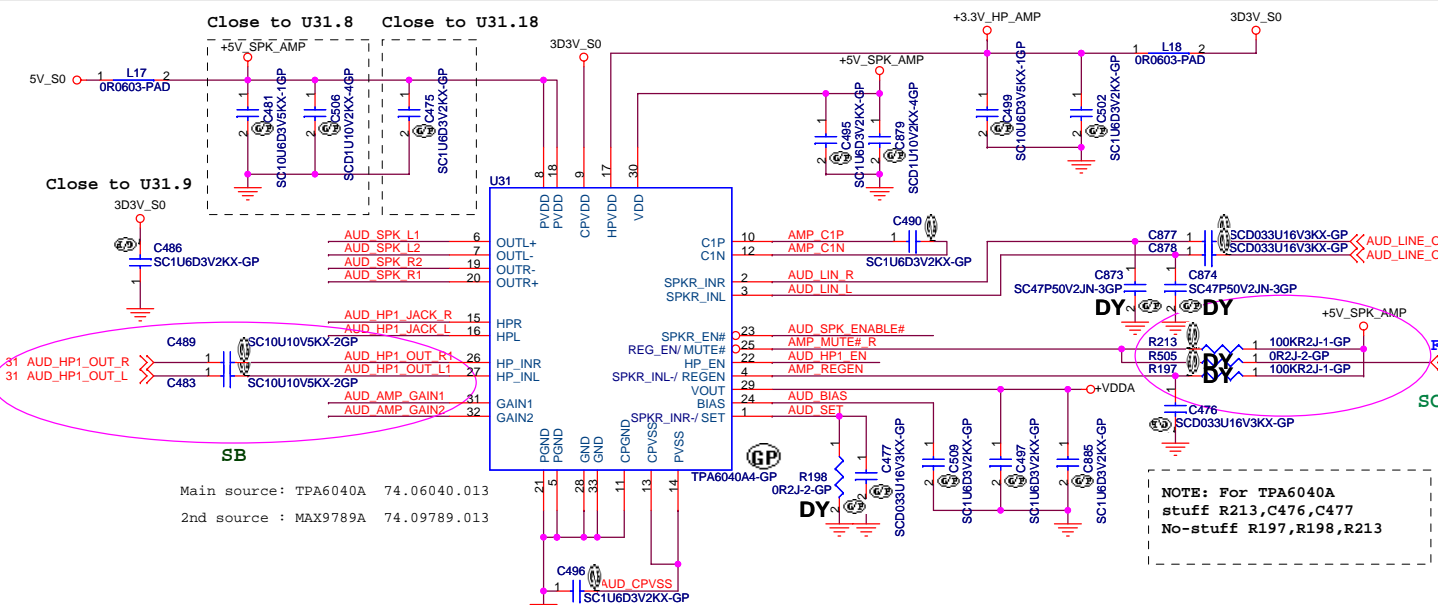
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

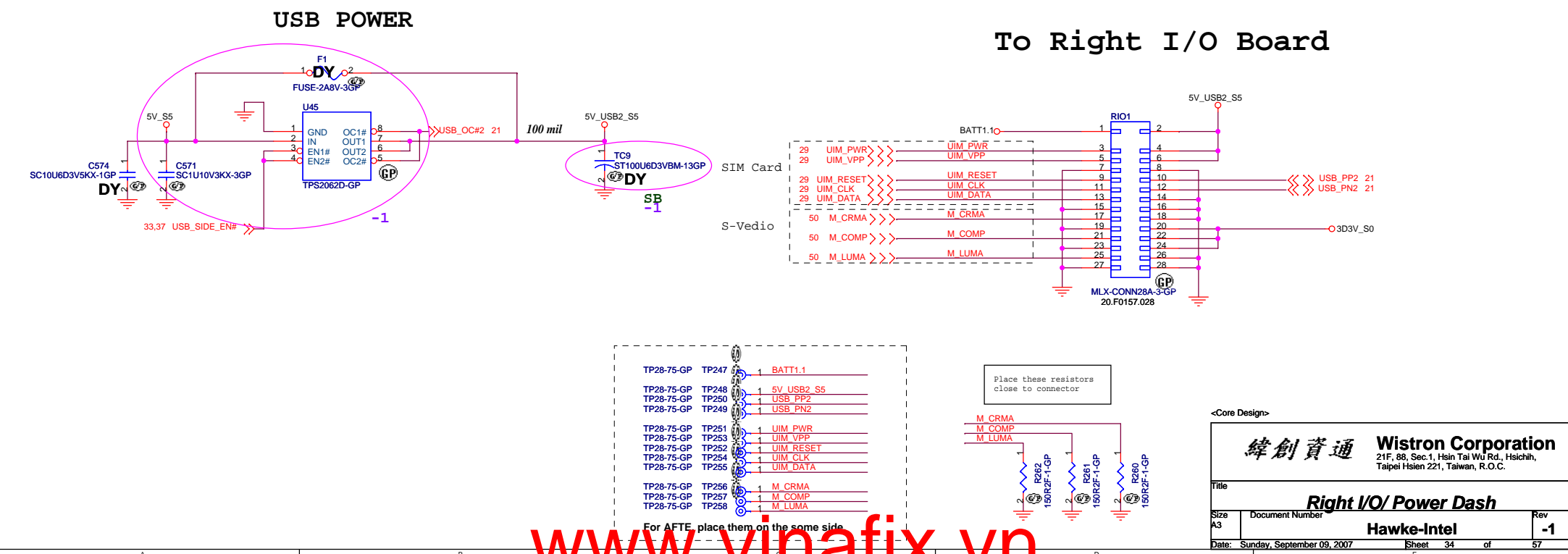
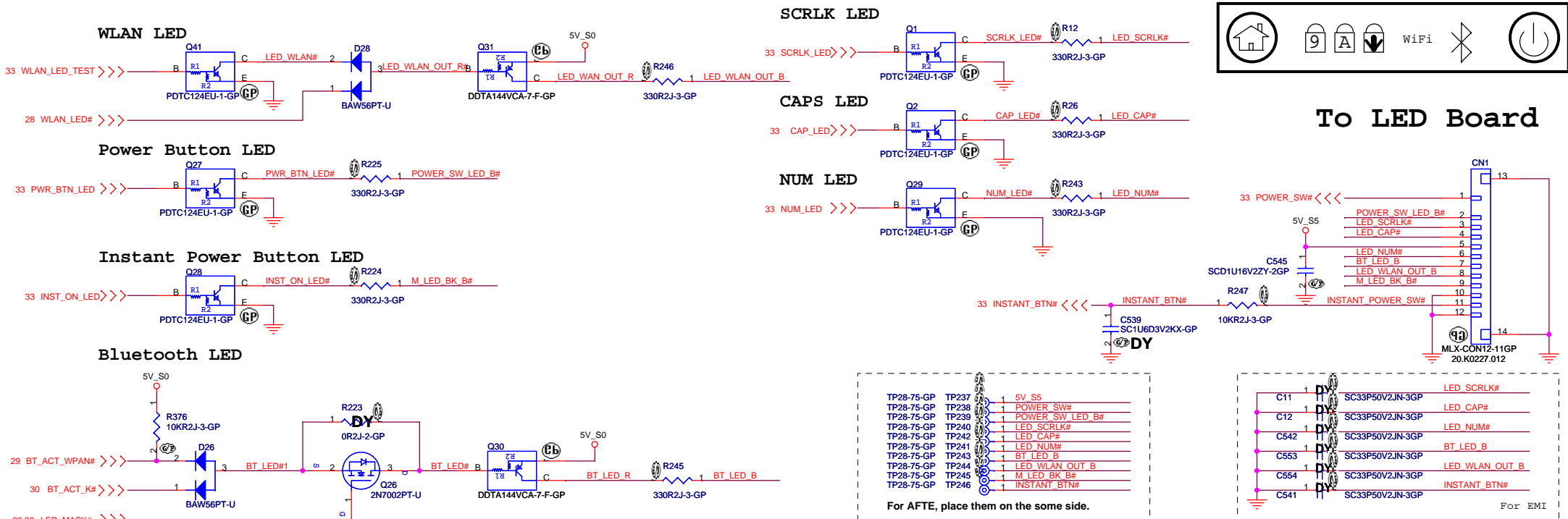
Title **AUDIO CODEC STAC9228**

Size A3 Document Number **Hawke-Intel** Rev **-1**

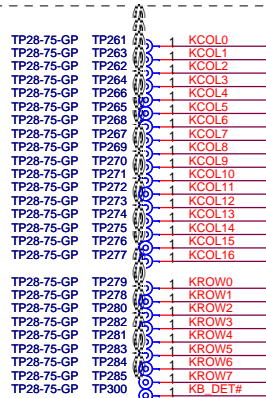
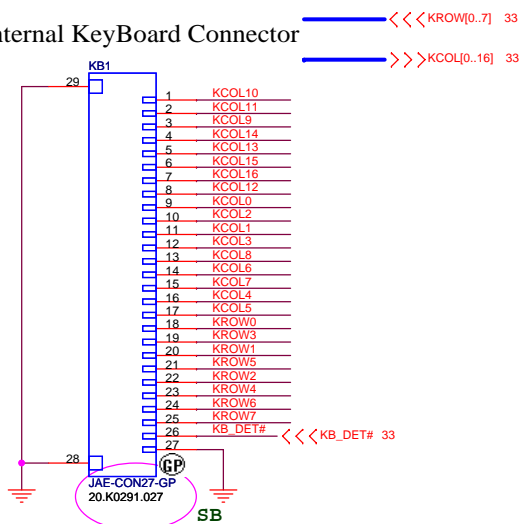
Date: Sunday, September 09, 2007 Sheet 31 of 57

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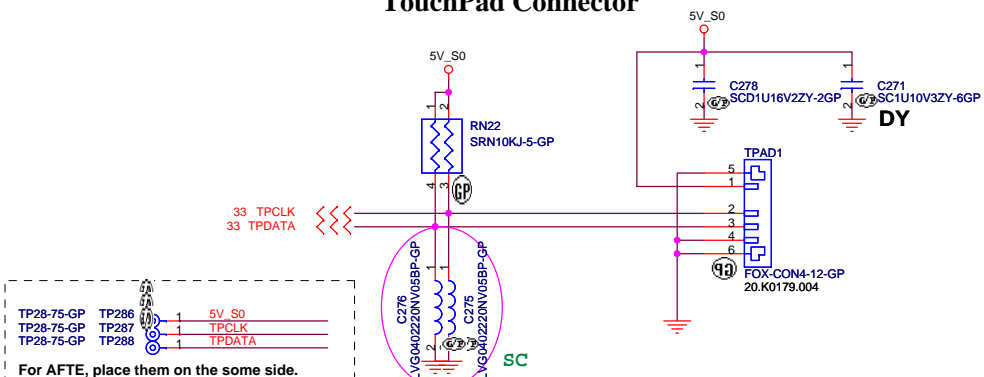


Internal Keyboard Connector



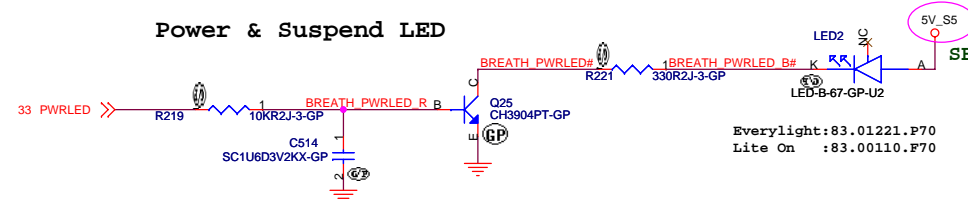
For AFTE, place them on the same side.

TouchPad Connector



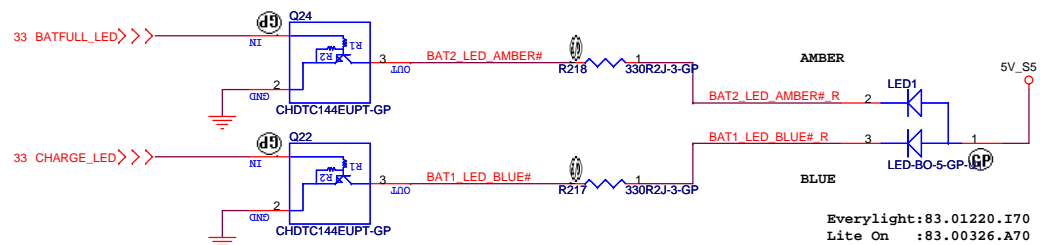
For AFTE, place them on the same side.

Power & Suspend LED



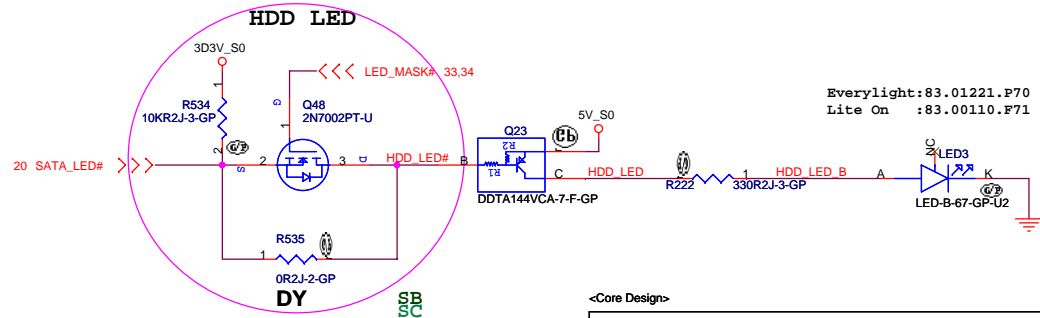
Everylight:83.01221.P70
Lite On :83.00110.F70

Battery LED



Everylight:83.01220.I70
Lite On :83.00326.A70

HDD LED



Everylight:83.01221.P70
Lite On :83.00110.F71

LED Board

LED NAME

ACTIVE SIGNAL

Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC)	
	WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini)	
	BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

Main Board

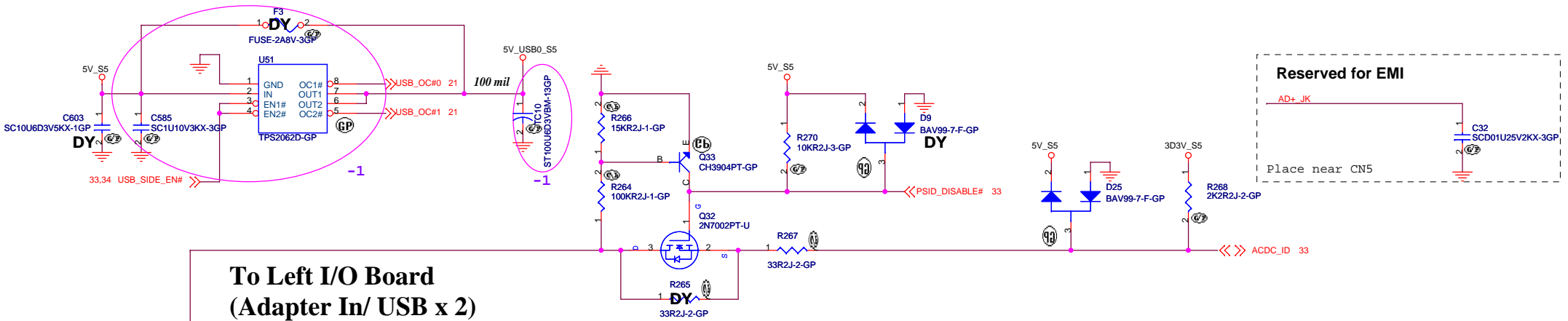
Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC)

<Core Design>

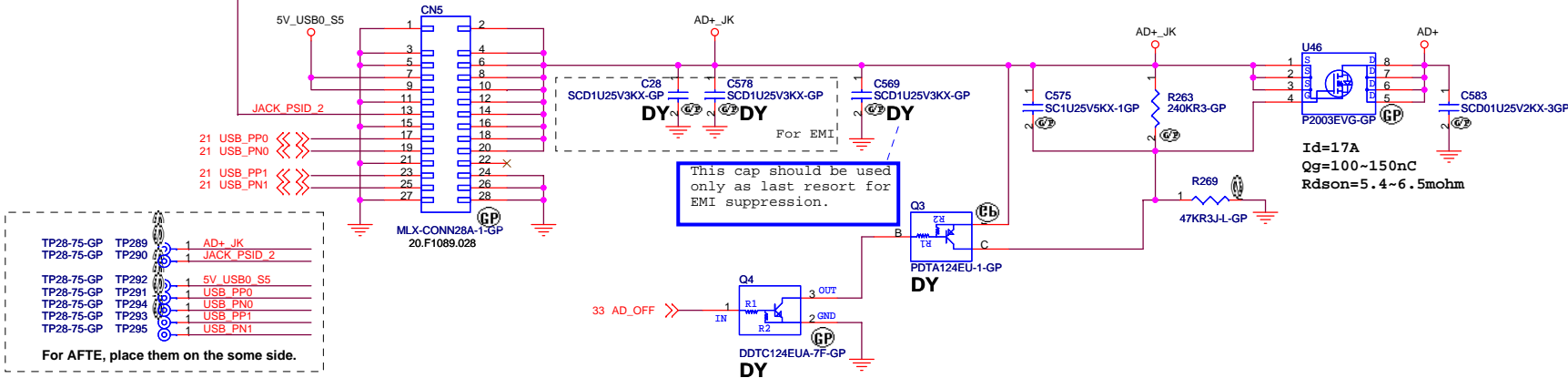
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Title	KeyBoard/Touchpad	
Size A3	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007	Sheet 36	of 57

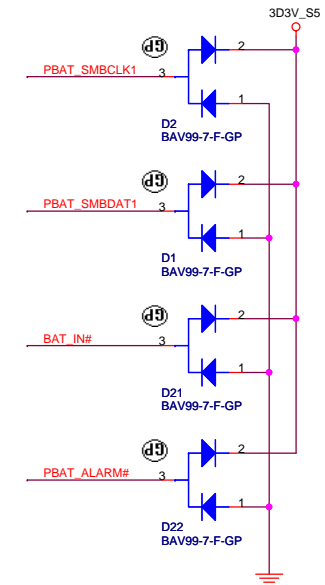
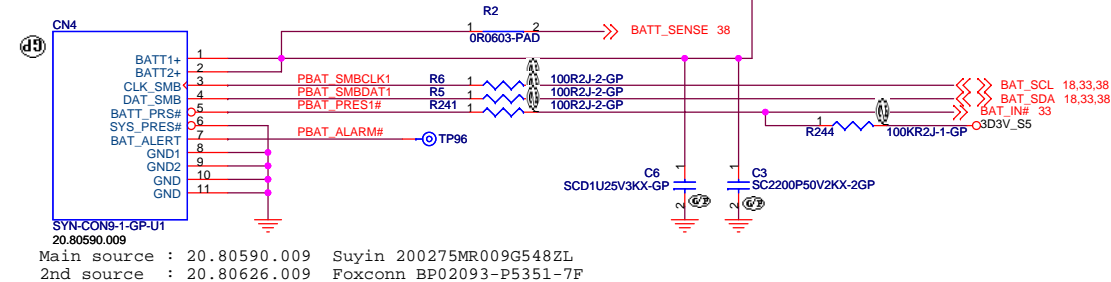
USB POWER



To Left I/O Board (Adapter In/ USB x 2)



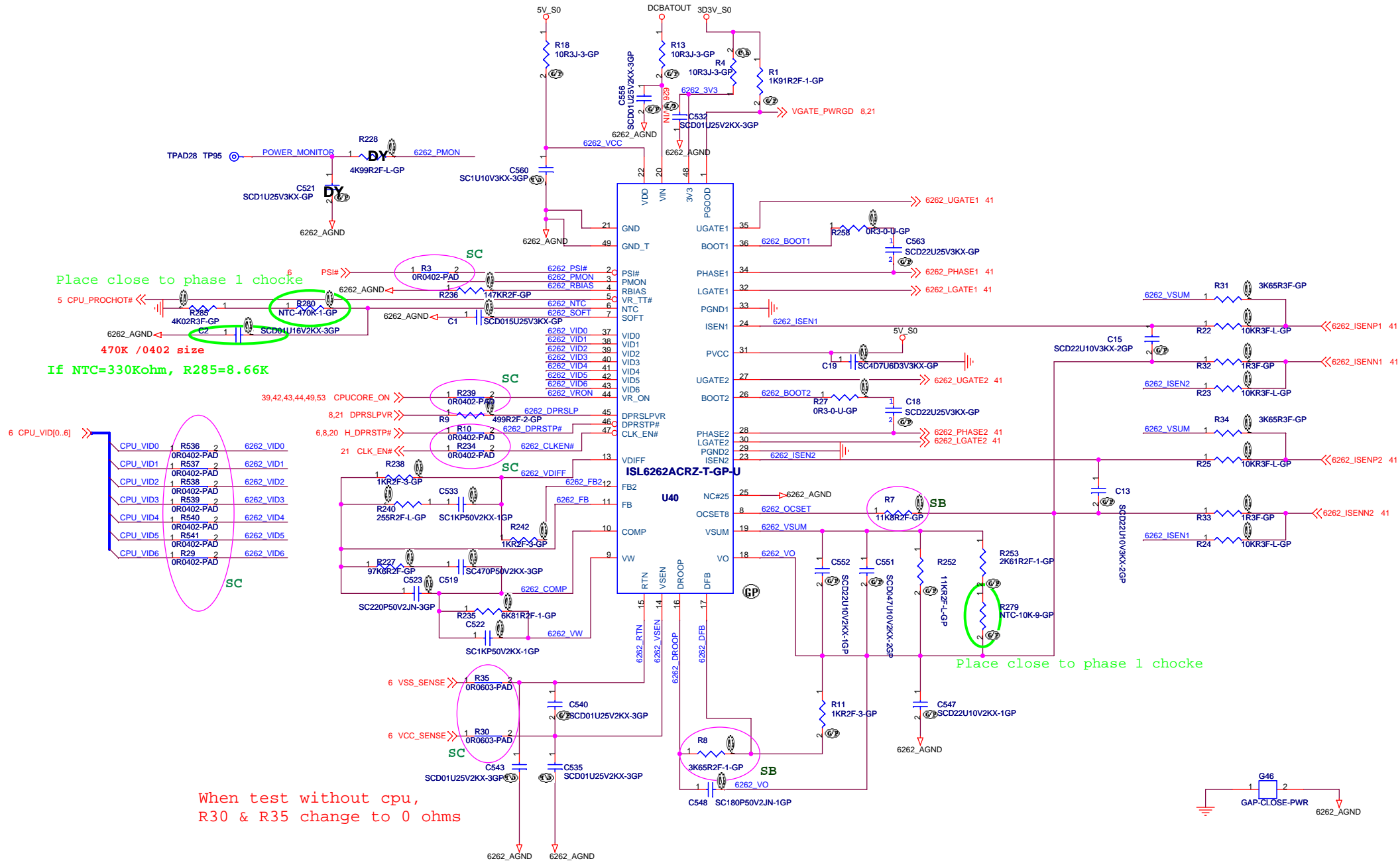
Batt Connector



<Core Design>

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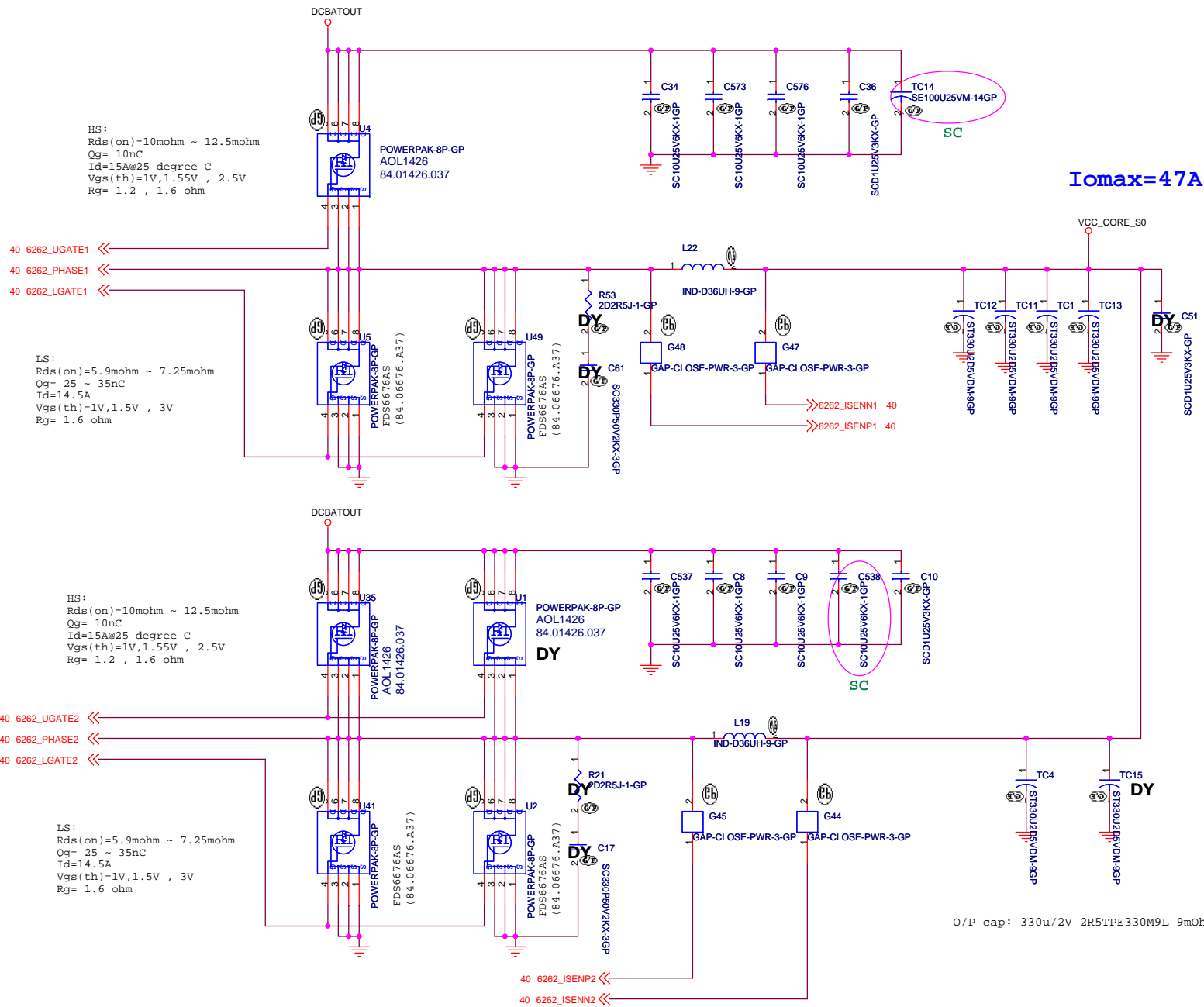
AD/BATT CONN		
Size A3	Document Number	Rev -1
Date: Sunday, September 09, 2007	Sheet 37 of 57	



<Core Design>

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Title			
DC-DC VCCCPUCORE 1/2			
Size	Document Number	Rev	
A3	Hawke-Intel	-1	
Date: Sunday, September 09, 2007		Sheet 40	of 57

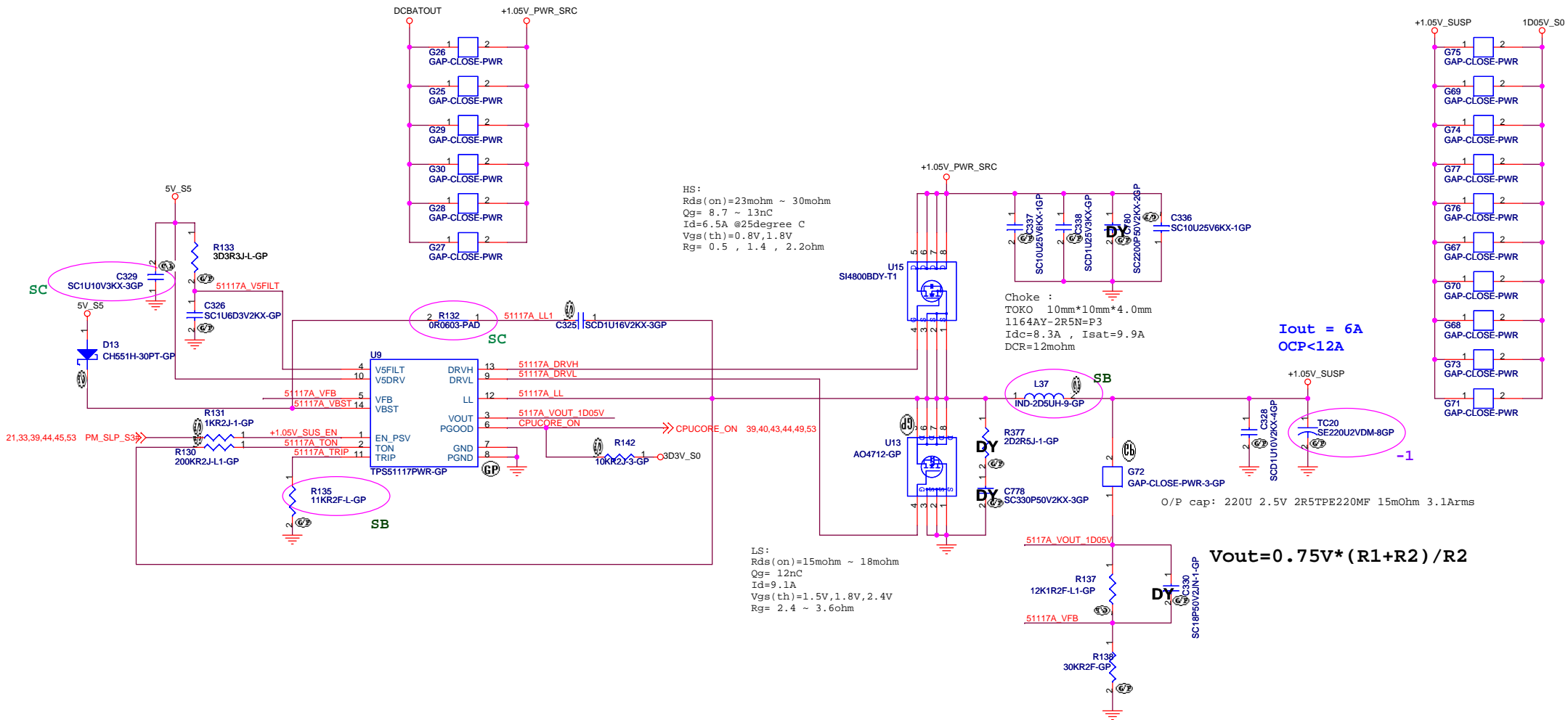


If VCC_SENSE and VSS_SENSE pins have pulled
 resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

<Core Design>

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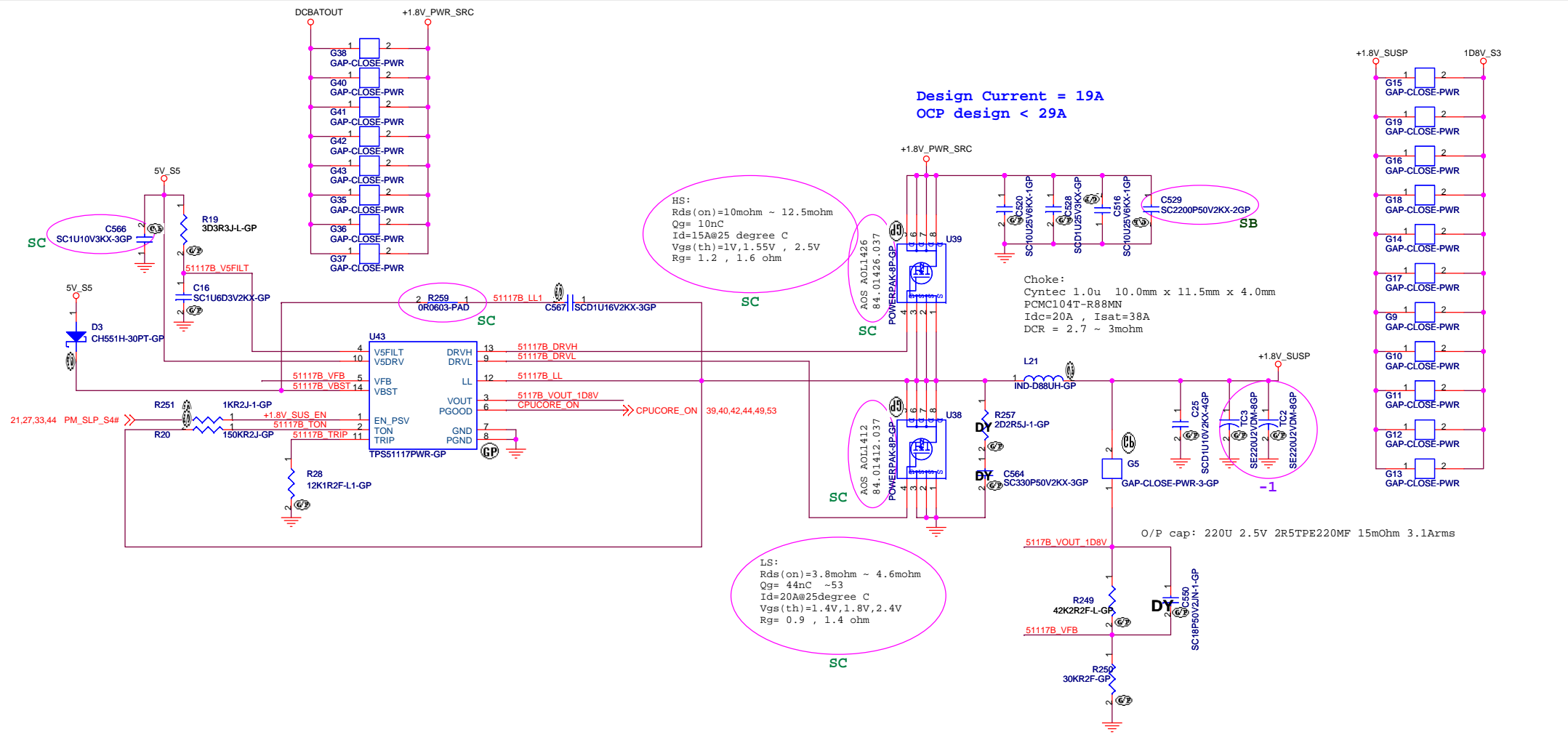
DC-DC VCCCPUCORE 2/2		
Size A3	Document Number	Rev -1
Hawke-Intel		
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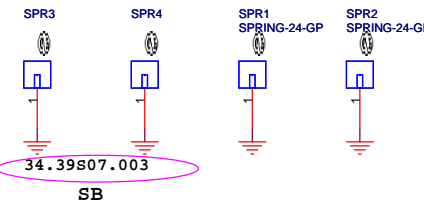
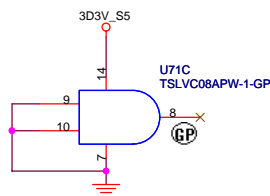
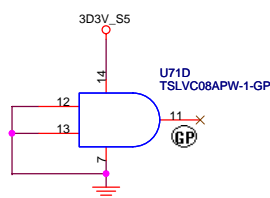
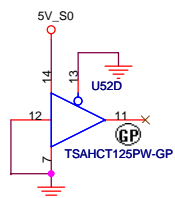
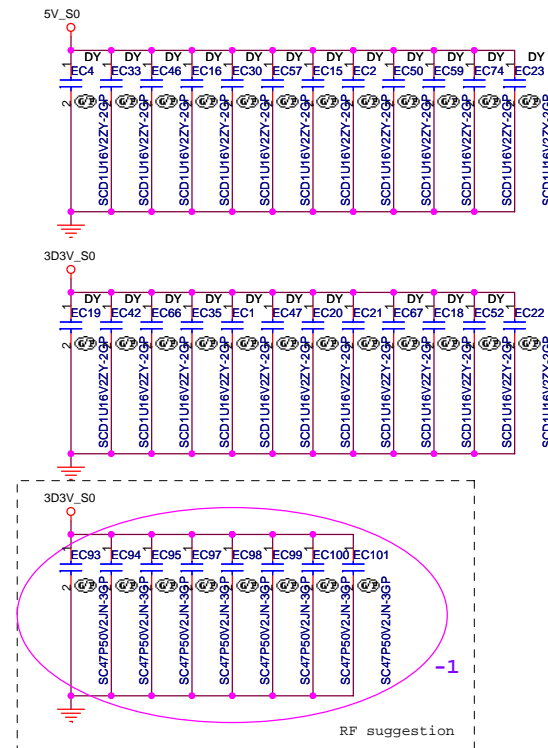
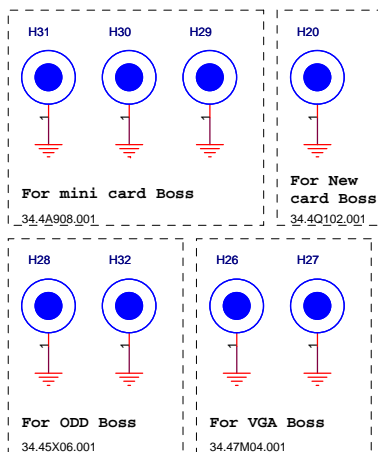
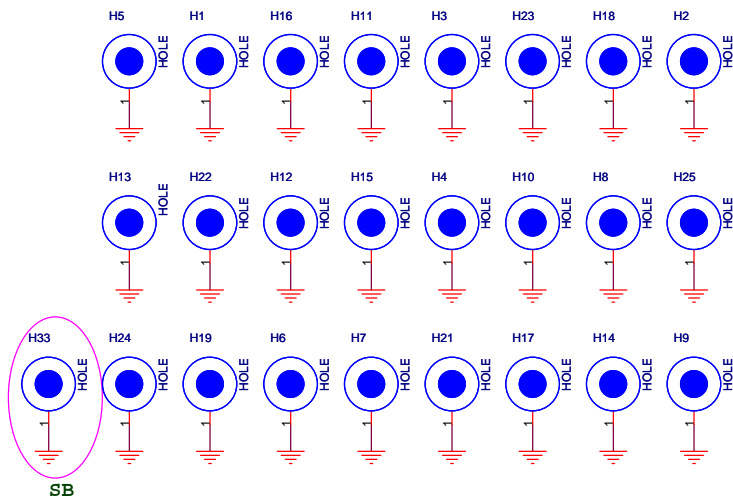
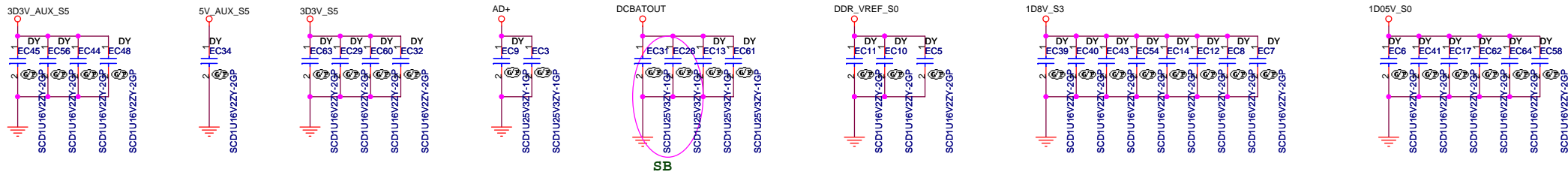
Title			DCDC 1.05V
Size	Document Number	Rev	
A3	Hawke-Intel	-1	
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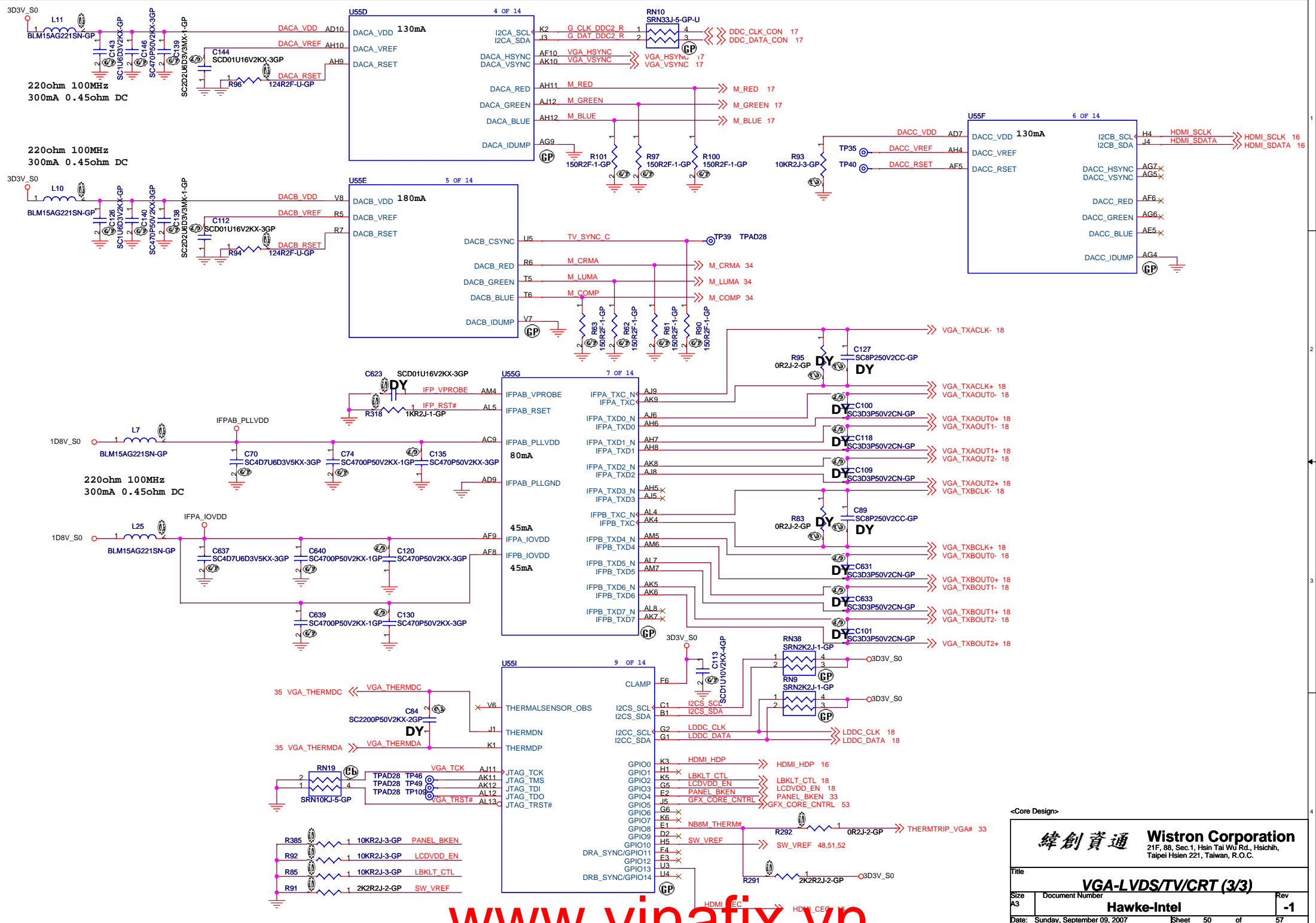


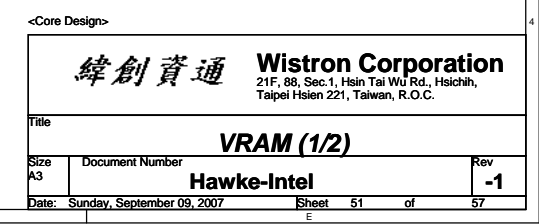
$$V_{out}=0.75V*(R1+R2)/R2$$

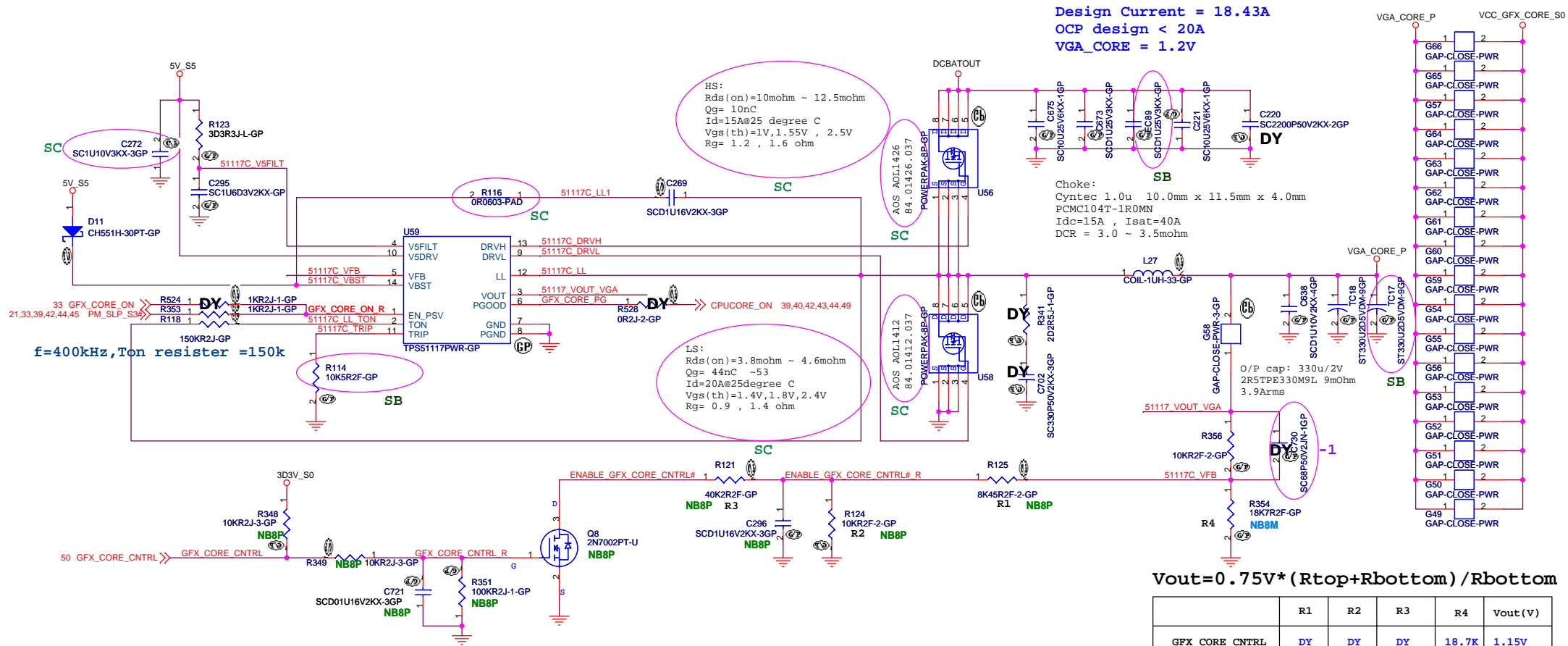
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Title	
DC/DC 1D8V(ISL6268)	
Size	Document Number
A3	Hawke-Intel
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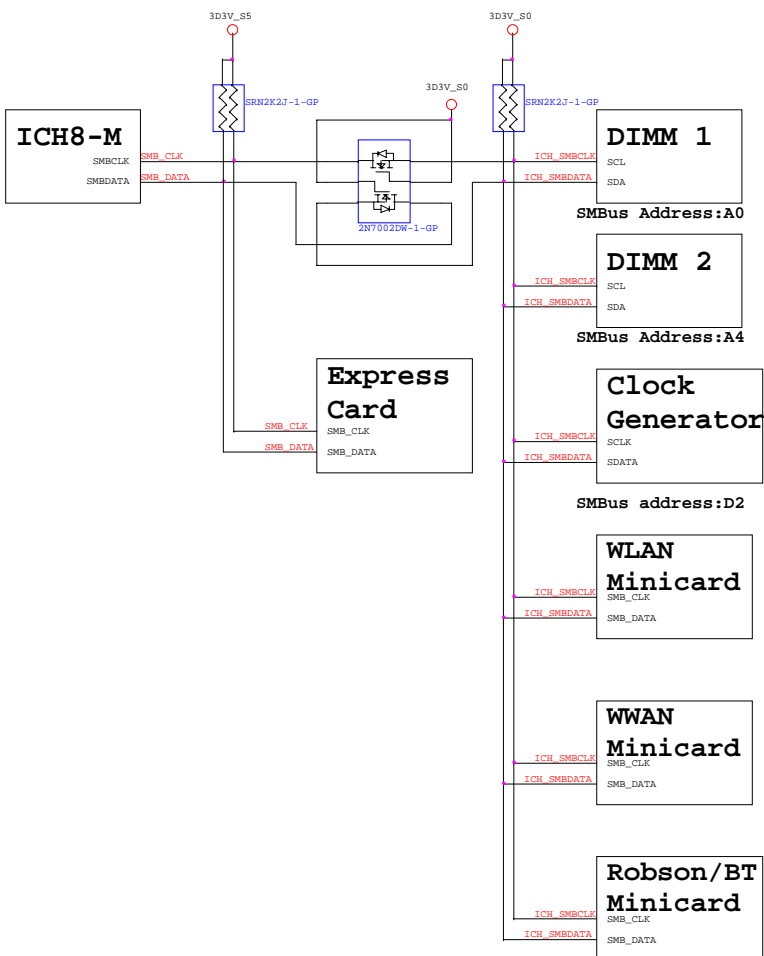




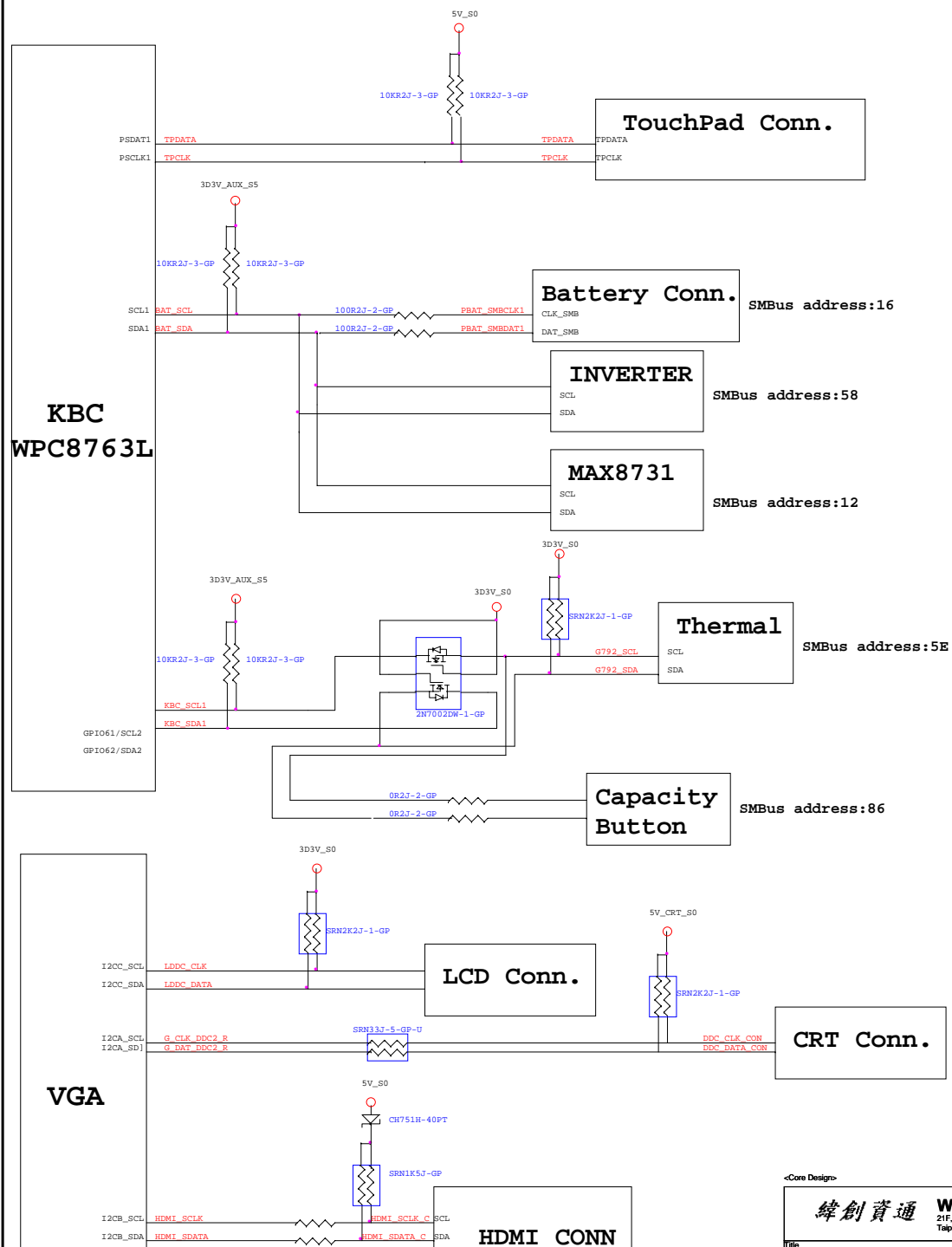




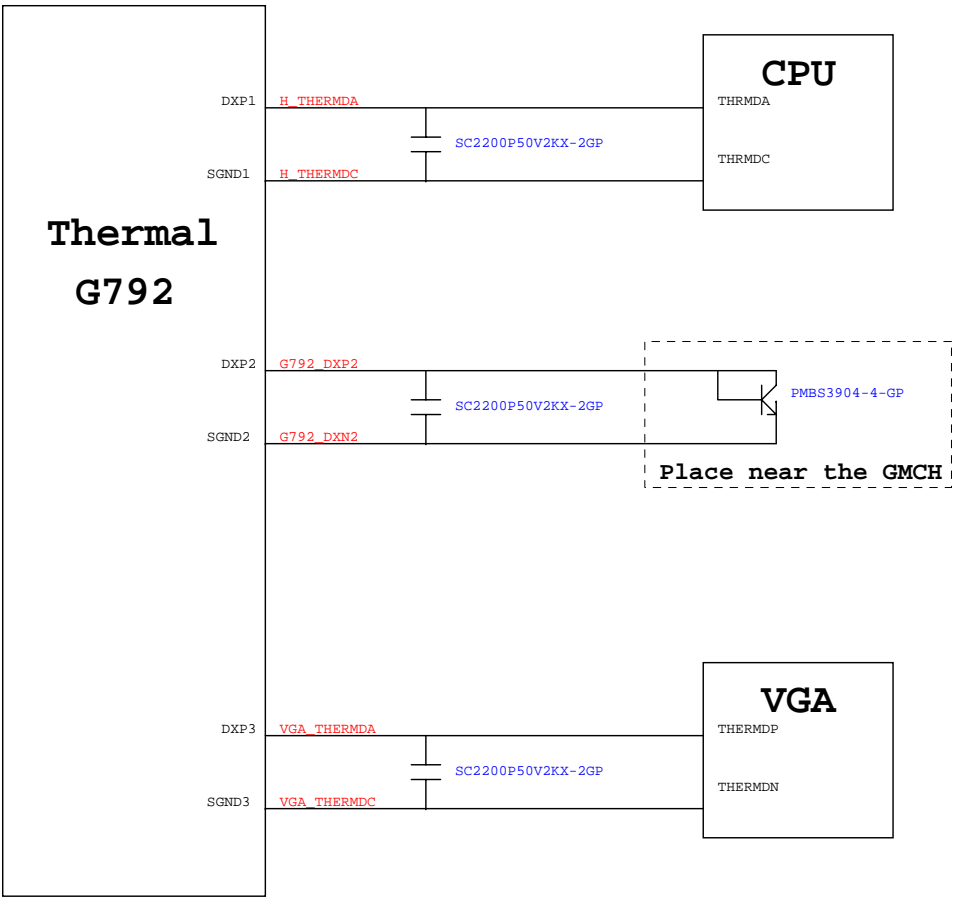
ICH8 SMBus Block Diagram



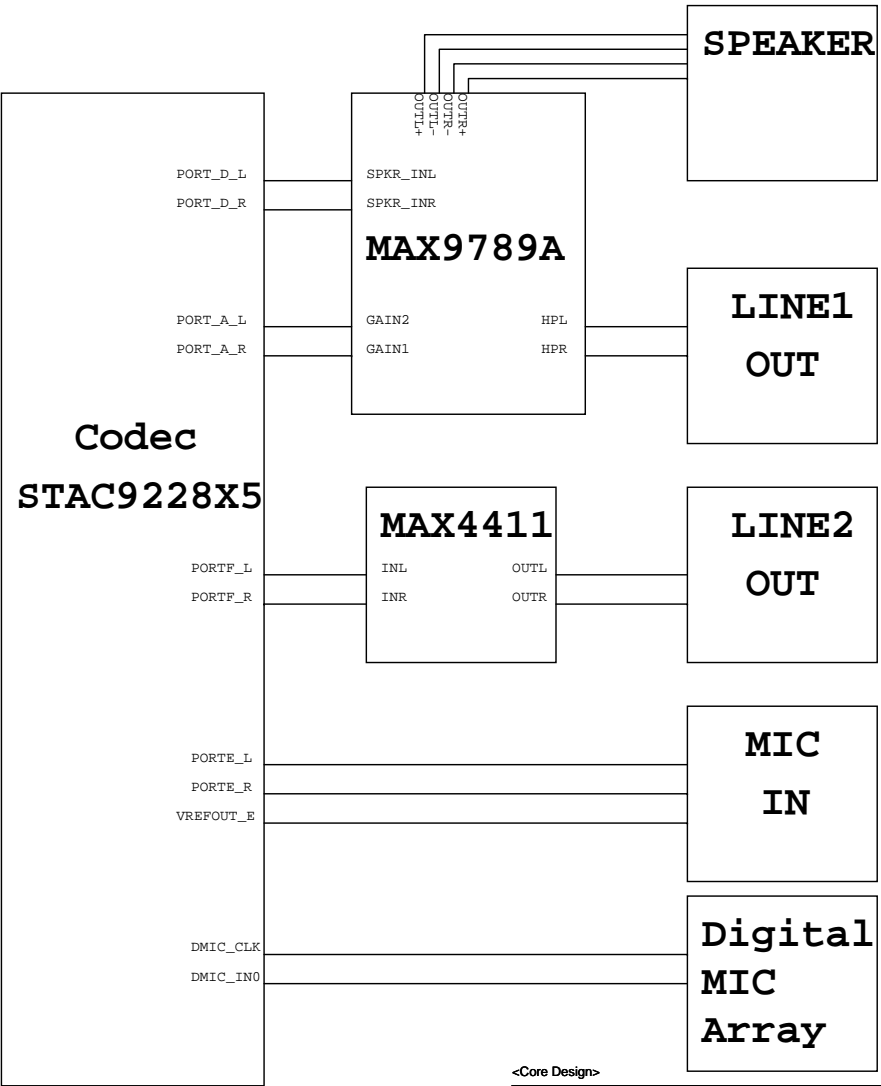
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/06	X00 to X01	1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
		15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

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HISTORY from X00 to X01

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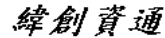
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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/08/17	X01 to X02	1	4	Changed U22 from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB singnal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Just keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
		14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

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